

# THÈSE

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## ABSTRACT

The market for photovoltaic systems has experienced a very high growth rate in recent years. This growth is mainly due to photovoltaic systems linked to the electricity distribution network. The disparity of voltage levels and currents between the sources (photovoltaic panels) and the electricity distribution network obviously requires high performance power converters.

The technical performance and reliability of converters are parameters that can significantly affect the production of electrical energy, the profitability and the financial costs of a system. These facts led to an international race for low profile power converters, which exposed several limitations to the use of conventional magnetic component structures. This last structure takes a volume of 70% in the power converter, which makes the integration of passive components an inevitable solution.

The objective of this thesis is to design power converters with very small sizes dedicated to the photovoltaic system by designing low profile magnetic passive components (inductor).

The work started with the implementation of the design and the dimension of the planar inductor model to be integrated in the DC-DC Boost converter, taking into account the specified space, which must not be exceeded. Following a comparison of planar coils of different shapes, we opted for the square geometry. This coil has been improved to take advantage of mutual inductance. Thus, we designed a dual-layer inductor. In-depth studies were carried out in order to opt for the optimal conductor thickness and the width of the gap. These parameters are two very disturbing elements and generate significant energy losses. It should be noted that the thickness of the conductor was neglected by the literature and does not appear in any formula to the calculation of the inductance value.

The design of an equivalent circuit of the dual-layer inductor has validated its correct operation and that of the converter which contains it.

To correct the drop in the converter's output voltage, we designed a corrector block that keeps it constant. This block, allowed us to designed a smart converter which stabilizes automatically, its output voltage whatever the input voltage coming from the PV module.

The study of electromagnetic and thermal behaviour is an essential operation in designing of our dual-layer inductor.

The results obtained by different simulation using COMSOL Multiphysics confirmed that a very thin conductor thickness and too narrow gap between the two stacked coils of the dual layer inductor are not recommended

## RESUME

Le marché des systèmes photovoltaïques a connu un taux de croissance très élevé ces dernières années. Cette croissance est principalement due aux systèmes photovoltaïques reliés au réseau de distribution d'électricité. La disparité des niveaux de tension et des courants entre les sources (panneaux photovoltaïques) et le réseau de distribution électrique nécessite évidemment des convertisseurs de puissance performants.

Les performances techniques et la fiabilité des convertisseurs sont des paramètres qui peuvent affecter significativement la production d'énergie électrique, la rentabilité et les coûts financiers d'un système. Ces faits ont conduit à une course internationale pour les convertisseurs de puissance à profil bas, qui a exposé plusieurs limitations à l'utilisation de structures de composants magnétiques conventionnelles. Cette dernière structure prend un volume de 70% dans le convertisseur de puissance, ce qui fait de l'intégration de composants passifs une solution incontournable.

L'objectif de cette thèse est de concevoir des convertisseurs de puissance de très petites tailles dédiés au système photovoltaïque en concevant des composants passifs magnétiques à profil bas (inductance).

Le travail a commencé par la mise en œuvre de la conception et de la dimension du modèle d'inductance planaire à intégrer dans le convertisseur DC-DC Boost, en tenant compte de l'espace spécifié, qui ne doit pas être dépassé. Suite à une comparaison de bobines planaires de différentes formes, nous avons opté pour la géométrie carrée. Cette bobine a été améliorée pour tirer parti de l'inductance mutuelle. Ainsi, nous avons conçu une inductance à double couche. Des études approfondies ont été menées afin d'opter pour l'épaisseur optimale du conducteur et la largeur de l'entrefer. Ces paramètres sont deux éléments très perturbateurs et génèrent des pertes d'énergie importantes. Il est à noter que l'épaisseur du conducteur a été négligée par la littérature et n'apparaît dans aucune formule permettant le calcul de la valeur de l'inductance.

La conception d'un circuit électrique équivalent de l'inducteur double couche a validé son bon fonctionnement et celui du convertisseur qui la contient.

Pour corriger la chute de tension de sortie du convertisseur, nous avons conçu un bloc MPP qui la maintient constante. Ce bloc MPP, nous a permis de concevoir un convertisseur intelligent qui stabilise automatiquement sa tension de sortie quelle que soit la tension d'entrée provenant du module PV.

L'étude du comportement électromagnétique et thermique est une opération essentielle dans la conception de notre inductance bicouche.

Les résultats obtenus par différentes simulations à l'aide de COMSOL Multiphysics ont confirmé qu'une épaisseur de conducteur très mince et un espace trop étroit entre les deux bobines empilées de l'inducteur à double couche ne sont pas recommandés.

## ملخص

شهد سوق الأنظمة الكهروضوئية معدل نمو مرتفعاً جداً في السنوات الأخيرة. ويعود هذا النمو بشكل رئيسي إلى الأنظمة الكهروضوئية المتصلة بشبكة توزيع الكهرباء. من الواضح أن التباين في مستويات الجهد والتيارات بين المصادر (الألواح الكهروضوئية) وشبكة التوزيع الكهربائي يتطلب محولات طاقة فعالة. يعد الأداء التقني وموثوقية المحولات من العوامل التي يمكن أن تؤثر بشكل كبير على إنتاج الطاقة الكهربائية والربحية والتكاليف المالية للنظام. أدت هذه الحقائق إلى سباق دولي لمحولات الطاقة منخفضة المستوى، والتي كشفت العديد من القيود على استخدام هياكل المكونات المغناطيسية التقليدية. يشغل هذا الهيكل الأخير 70٪ من حجم محول الطاقة، مما يجعل تكامل المكونات السلبية حلاً أساسياً.

الهدف من هذه الأطروحة هو تصميم محولات طاقة صغيرة جداً مخصصة للنظام الكهروضوئي من خلال تصميم مكونات مغناطيسية سلبية منخفضة الارتفاع (محث) مع مراعاة المساحة المحددة التي لا ينبغي تجاوزها

بدأ العمل بتنفيذ تصميم وأبعاد نموذج الحث المستوي ليتم دمجها في المحول. بعد مقارنة المكثفات المستوية ذات الأشكال المختلفة، اخترنا هندسة المربع. تم تحسين هذا المكثف للاستفادة من الحث المتبادل ثم، قمنا بتصميم محث ذو طبقة مزدوجة. تم إجراء دراسات مكثفة من أجل اختيار السماكة المثلى للموصل وعرض الفجوة بين الملفين المتطابقين. تعتبر هذين المعلمين عنصرين ضارين للغاية ويولدان خسائر كبيرة في الطاقة. وتجدر الإشارة إلى أن الأدبيات أهملت سمك الموصل ولا يظهر في أي صيغة تسمح بحساب قيمة المحاثات.

لقد تم تصميم الدائرة الكهربائية المكافئة للمحث مزدوج الطبقة وتأكدنا من صحة تشغيله وتشغيل المحول الذي يحتوي عليه..

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# General Introduction

## General Introduction

Photovoltaic energy is currently experiencing substantial development in the world and in Algeria. This development is doped by international and national policies aimed at decreasing the use of fossil energies according to the objectives of the 2021 United Nations Climate Change Conference (COP26).

In its new energy policy, the Algerian government has implemented several measures to develop the renewable energy industry. The objective of this new policy is to make the renewable industry, especially solar energy, economically viable and competitive with fossil fuels. Algeria took a big step regarding clean energies by committing to a new challenging program for sustainable energy. In its updated version, these renewable energies program consists of installing a renewable power in the order of 4 GW by 2024 for the national market, with the maintenance of the export option as a strategic goal.

The photovoltaic field topologies used previously for isolated network facilities and low powers are unsuitable for this new development. The powers are essential, shading problems are highlighted, and the return time becomes capital. Under these conditions, photovoltaics field topologies must be modified to satisfy these new needs.

Recent developments in photovoltaic field topologies show an increasingly important insertion of power electronics. The PV topologies with central inverters fail regarding their performance and maintaining process compared to topologies with power optimizers or micro-inverters. Even resorting to modular topologies with micro-inverters or power-optimizers, is not expected because of their high cost, especially for large-scale systems. Therefore, the integration of the passive components of these converters becomes an inevitable solution in order to solve the cost and profile problems.

The tendency in power converters toward high power density, high operating frequency, and low profile has revealed many constraints in the use of standard wire-wound magnetic element topologies. Planar inductors and transformers practically remove some inconveniences of traditional wire-wound kinds. As a result, planar magnetics has grown in popularity in high-frequency power converters at recent years.

The work presented in this thesis deals with the miniaturization of a Boost DC/DC converter dedicated for photovoltaic applications, as well as the improvement of its performances. Our main objective is to design chopper of very small size which can be inserted at the back of the PV module. This chopper is equipped with an autonomous correction system which allows it to correct automatically its output voltage and maintain it stable regardless of the voltage received from the PV panel. Reducing the size of a chopper seems very simple, but in reality, it is a heavy work that requires multidisciplinary research involving power integration, materials science, the physics of magnetism, thermal, characterization and modelling, without forgetting production processes.

The miniaturization of the converter goes through the miniaturization of its passive components which occupy 80% of its volume. The chosen converter works under an operating frequency of 500 KHz, receives an input voltage of 17V to convert it into a 220 V voltage.

This thesis includes 5 chapters, in the first chapter, we present in a first part generalities on the cells and the photovoltaic systems. We recall the basic structure of a PV cell, its operating principle, its electrical characteristics, as well as the different arrangements of static converters in photovoltaic systems. The second section of this chapter outlines the current state of the art integration of passive components, in particularly the planar magnetic structures.

Chapter 2 has established the concept and sizing of the integrated planar inductor model for the DC-DC boost converter. we were interested at the dimensioning of the conductor thickness of the inductor which plays a crucial role in energy losses and the control the heating of the inductor. We have investigated for different thicknesses, the behaviour of the series resistance, quality factor, power losses, current density, inductance and leakage current using numerical simulation.

In Chapter III, we have discussed the geometrical dimensioning and electrical modelling of a dual-layer inductor which is more improved than the single-layer inductor. This dual-layer inductor will be integrated in our boost DC-DC converter dedicated fo PV systems.

To achieve a good geometrical dimensioning of the dual-layer inductor without degrading its performances, we have studied the influence of the gap (between the two stacked coils) and the conductor thickness on several important parameters: series resistance, quality factor, power losses, current density, inductance, and leakage current. This study has shown that these two parameters have a significant effect on the inductor's performances.

In chapter IV, our objective is to investigate the DC-DC boost converter's behaviour and performances with the different dual-layer inductors resulting from the previous chapter.

First, we validated the proper functioning of our converter containing a perfect classic coil. To test the operation of the dual-layer inductor, we designed its electrical circuit which we integrated into the circuit of the Boost converter. Using the PSIM simulation software, we have visualized the different waveforms of the currents and voltages of the converter for different gaps and different conductor thicknesses. The waveforms were consistent with those of the literature and the measured values of the output voltages from the different gaps and thicknesses varied between 204.5V and 216.4V. Knowing that the target voltage is 220V, these values therefore need to be adjusted. To do this, we have designed a duty cycle corrector block that we have integrated into the Boost converter. This idea allowed us to design a smart converter which regulates its output voltage by varying its duty cycle.

The values of the output voltages measured after correction, varied between 220.07V and 220.17V. These results are very satisfactory. The idea behind the design of this smart converter is to keep a stable output voltage regardless of the input voltage coming from the solar panel. Because the voltage coming from the PV panel is never stable due to the parameters of shading, dust, etc.

A good simulated output voltage does not guarantee the proper functioning of the dual-layer inductor, because during its operation other effects may arise, such as overheating of the inductor, or saturation of the core, etc. To reach the final choice of the conductor thickness and the gap, we will move on to electromagnetic and thermal simulations.

The reduction of volume in a magnetic component leads to many problems such as, magnetic core saturation, important heat flux, high leakage currents and others. So, these problems need to be resolved to guarantee the proper functioning and reliability of the component.

To validate the choice of the optimal conductor thickness and the optimal gap, we have studied in chapter V the electrical and magneto-thermal behaviour of the dual-layer inductor for different thicknesses and different gaps. This study was made by using the COMSOL Multiphysics simulation software.

To study skin and proximity effect phenomena, we have visualized the distribution of the current density inside the conductor. To ensure that the magnetic behaviour of our inductor does not adversely impact the neighbourhood components, we have visualized the distribution of the field lines and the magnetic flux. For the thermal component, we had to make sure that the operating temperature of the dimensioned inductor was within the standards and that it was uniformly distributed. Therefore, we have visualized the temperature distribution for different conductor thicknesses and different gaps.

These simulations have shown that a very thin winding is not recommended and a very small gap generates a lot of leakage currents between the two stacked coils of the dual-layer inductor. We have also noticed through these simulations that the dual-layer inductor has the lowest temperature at its centre, unlike single layer inductors where the highest temperature is recorded at their centres.

These simulations were very beneficial to us in avoiding some defects and designing a dual-layer inductor with very small dimensions, capable of operating correctly with better efficiency.

This research work ends with a general conclusion.

# Chapter I

Photovoltaic Topologies and Integrated  
Magnetic for Power Converters



## **1. INTRODUCTION**

A group of American researchers from Bell Labs constructed the first cell capable of converting solar energy into electric current one hundred years after Edouard Becquerel discovered the photovoltaic phenomenon in 1839 [1-2]. The photovoltaic effect was initially understood in the space sector before being employed as a source of energy at the isolated site and to know the progress we are witnessing now in applications connected to the network. This market penetration was accompanied by an increase in yield, 4% for Bell Labs cell, nearly 42% for the World Record.

In the first section of this chapter, we will look at the photovoltaic sector in its broadest sense. To characterise the modes of functioning of PV cells, we shall determine their properties and model them. Then, we'll look at their interconnections and the safety devices that will be used while running a module or a PV field. Understanding how a PV generator works will enable us to comprehend the critical effects resulting from the interconnection of PV generators with different characteristics (mismatch) on production. We will discuss the various cell technologies employed, stressing their advantages and disadvantages.

In the second part, we will discuss the state of the art of integration technology of passive components (specifically, the inductors), their constraints and their limits, the fields of inductors application, the materials used in integration, the technological methods of manufacturing of integrated inductors, also the improving methods of the quality factor.

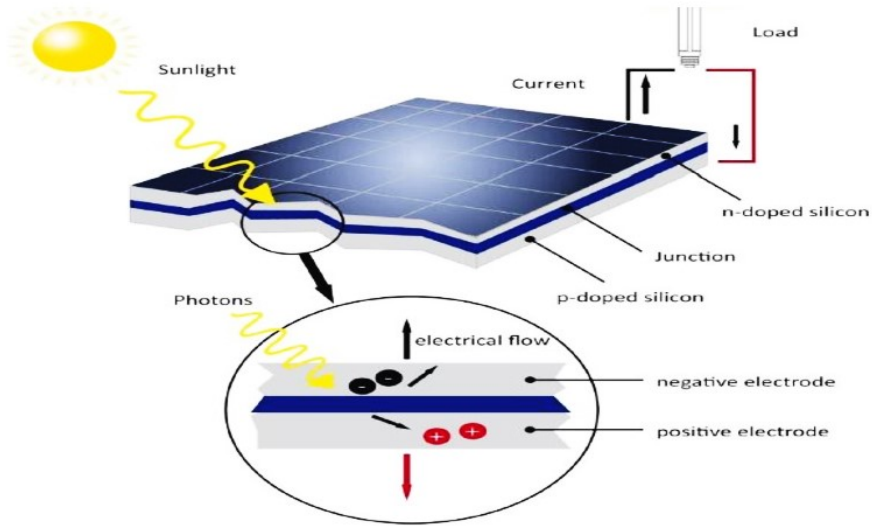
## **2. PHOTOVOLTAIC ENERGY**

### **2.1. The photovoltaic cell**

A photovoltaic cell is an energy harvesting device that turns solar energy into usable electricity via a process known as the photovoltaic effect. PV cells come in various shapes and sizes. They always rely on semiconductors to interact with incoming photons from the Sun to create an electric current [3-7]. We will quickly present the operation of the photovoltaic effect.

### **2.2. The photovoltaic effect**

The functioning of the PV cell is based on a physical phenomenon called the photovoltaic effect. Figure I.1 illustrates the cut of a PV cell [8].

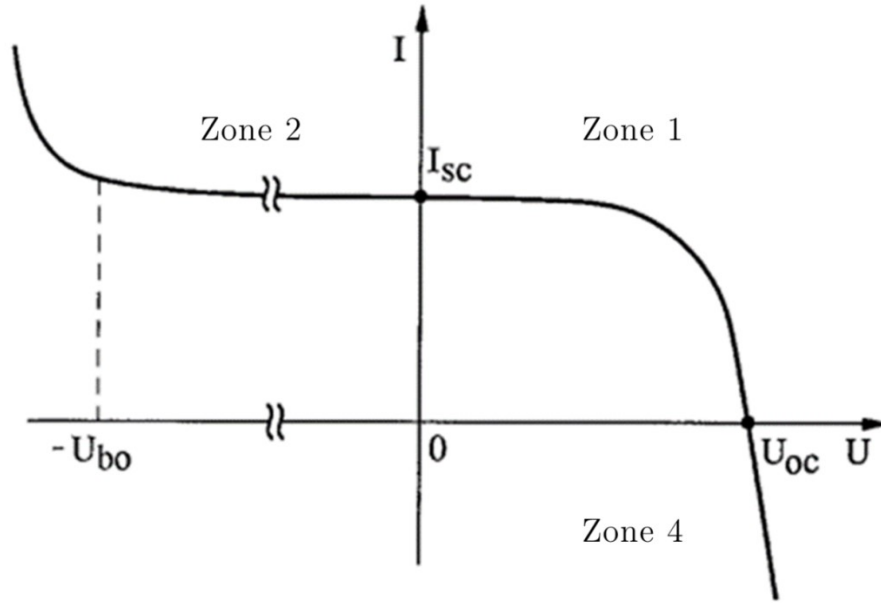


**Figure I. 1 : Solar cells working principle**

A photovoltaic cell is made from a silicon semiconductor material. Its construction is comparable to a conventional diode. The cell is made up of two different semiconductor layers. The upper layer is N-doped, and the lower layer is P-doped, thus creating a PN junction. This PN junction creates a potential barrier. When light reaches the PN junction, the light photons can easily enter in the junction, through very thin P-type layer. The light energy, in the form of photons, supplies sufficient energy to the junction to create a number of electron-hole pairs. This potential difference creates an E field which drains the free carriers to the metal contacts of the P and N regions. It results an electric current and a potential difference in the PV cell. The current and voltage supplied by a PV cell depend on various parameters that we will explain later [9-10].

### **2.3. Electrical characteristic**

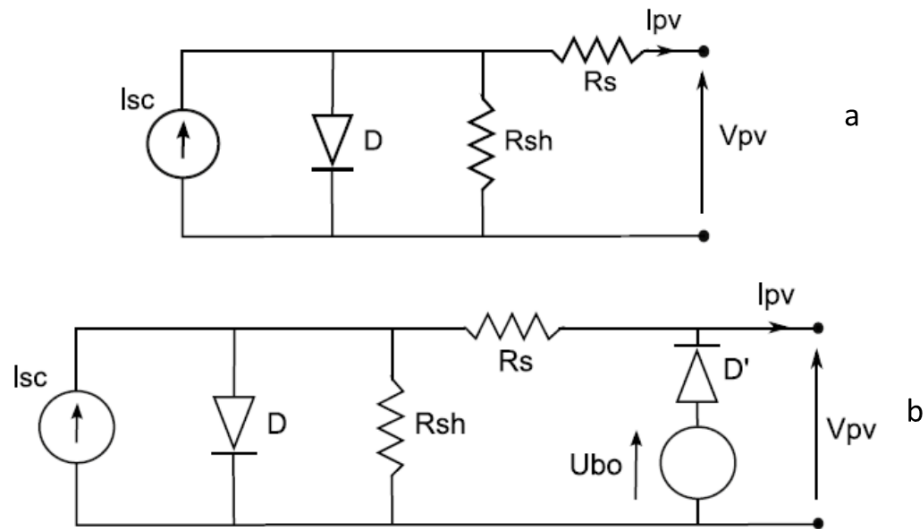
The photovoltaic cell has a non-linear  $I(V)$  characteristic (Figure I.2). The characteristic of a photovoltaic cell considers three quadrants on the existing 4 [11]. A PV cell is a receiver in zone 2 and zone 4. The operation in these two quadrants is to be avoided because the risk of destruction by the phenomenon of local heating (hot spot) is possible. The operation in zone 1 is the regular operation. In this case, the cell is a generator producing energy. The goal is to make the cell work in this quadrant.



**Figure I. 2:** I (V) Characteristic of a photovoltaic cell [2]

The open-circuit voltage ( $V_{oc}$ ) of a PV cell is between 0.3V and 0.7V depending on the material used, the temperature, and its state of aging. Its short-circuit current ( $I_{sc}$ ) varies mainly according to the illumination level and according to the technologies and the cell sizes (between 5 and 8A for crystalline silicon). A PV cell can be modelled by the schematics shown in Figure I.3.

Figure 1.3a models the PV cell in the first and fourth zones. A fourth branch is added in parallel to simulate the characteristic of the photovoltaic cell in the second zone (Figure 1.3b). This branch consists of a voltage generator  $U_{bo}$  ( $U_{bo}$  avalanche voltage) and a diode placed in series. It simulates the operation of the PV cell when reversing biased.



**Figure I. 3:** Equivalent circuit of a photovoltaic cell [2]

If the PV cell operates as a generator (zone 1), it produces a short-circuit current ( $I_{sc}$ ) proportional to the illumination. The output current equation in zone I (generating zone) in static is:

$$I_{pv} = i_{sc} - i_0 \left( e^{\frac{V_{pv} + I_{pv} R_s}{a}} - 1 \right) - \frac{V_{pv} + I_{pv} R_s}{R_{sh}} \quad \text{Equation (I. 1)}$$

This expression is directly related to the equivalent circuit of the cell in zone 1 [11-12]. With  $\alpha = KT/e$  where:

K: The Boltzmann constant ( $1.381 \times 10^{-23}$  J/k).

T: The temperature of the photovoltaic cell and e, the electron charge ( $e = 1.602 \times 10^{-19}$  C).

$I_{pv}$ : The current supplied by the cell in zone 1.

$V_{pv}$ : The voltage at the terminals of this same cell PV.

$i_0$ : The saturation current, and  $i_{sc}$  is the short circuit current of The PV cell.

$R_s$ : The series resistance linked to the different losses of connectors and contacts.

$R_{sh}$ : The shunt resistance characterizing the leakage currents of the cell

This static modelling of a polarized PV cell is very simple and can be easily implemented in the simulation tools. The limits of this model are the lack of modelling of cell dynamics and heating phenomena within the cell. Nevertheless, this model makes it possible to reproduce the main behaviours of a PV cell under the actual conditions of operation and its interactions with the other elements of the system. A dynamic model is developed in [13].

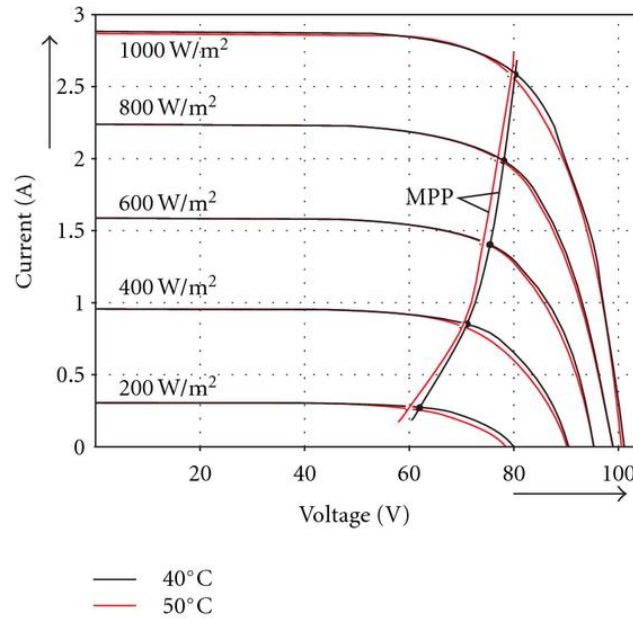
## **2.4. The influence of temperature and irradiation on the current-voltage characteristic**

### **2.4.1. Influence of irradiation**

The characteristic  $I(V)$  of a PV module is shown in figure I.4. For a fixed temperature, it is observed that the characteristic  $I(V)$  increases with the increase of irradiance. The same remark is made for the  $I_{sc}$  short-circuit current, while a small variation is observed for open-circuit voltage  $V_{oc}$  [14].

The characteristics of the PV generators are affected by the presence of partial shading (shading losses), in particular, the value of the maximum output power, the shape factor, and the efficacy of the PV generator. Therefore, it is very important to choose the appropriate

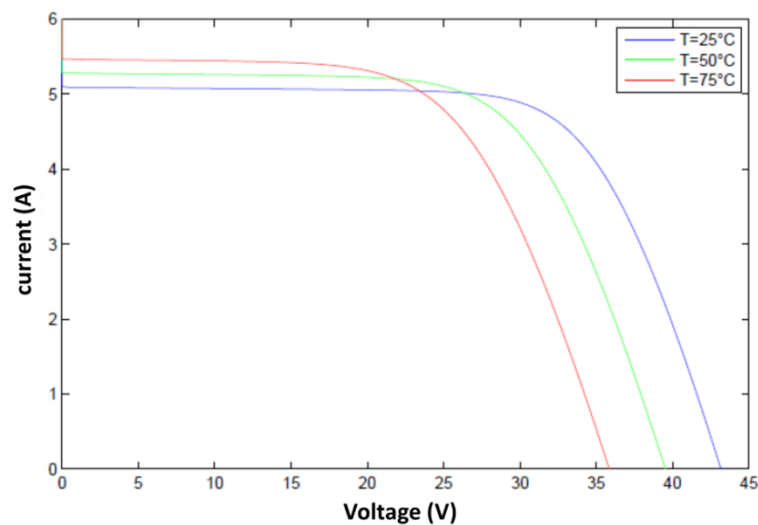
place for the PV generator to prevent the observation of partial shading during the operation of the PV installation.



**Figure I. 4:** Example of a network of characteristics of a photovoltaic generator for different irradiances [15]

#### 2.4.2. Temperature influence

For a fixed irradiance, the open-circuit voltage  $V_{OC}$  increases with the decrease in temperature (Figure 1.5), while a slight decrease is noticed on the short-circuit current  $I_{SC}$ . Decreasing saturation current  $I_0$  is the leading cause of current drop at low temperatures.



**Figure I. 5:** I(V) characteristic of the PV module for different temperatures

Therefore, temperature and irradiation are the two main parameters that will change the character of a PV generator. So, these two parameters will have to be carefully studied when setting up a PV installation.

A PV generator can operate optimally under low temperature and high irradiance. This is the case in an aeronautical application, for example [14].

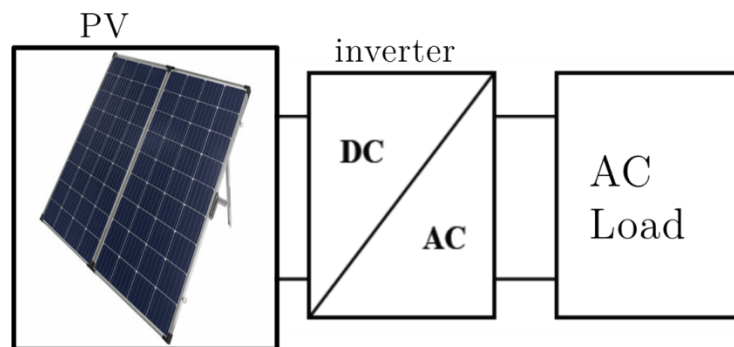
### 3. OVERVIEW ON SINGLE PHASE PV SYSTEMS

Single-phase PV systems have emerged as a viable option for supplying electricity to low-energy users (until 5 kW) [16-18]. These systems are employed in various settings, including residential and agricultural settings. The key advantages of these systems are their ease of deployment and low maintenance costs, which make them superior to other renewable energy systems (wind energy, thermal energy). Single-phase PV system topologies are classified into two groups based on the type of the provided load:

- 1- Single-stage PV systems;
- 2- Dual-stage PV systems.

#### 3.1. Single-stage: DC -AC converters

Because the majority of utilities are alternate, the usage of DC to AC converters (Inverters) becomes essential to secure energy transmission from the PV array to the AC utility. As illustrated in Figure I.6, these inverters might be beneficial for establishing a direct link between the PV panels and the AC utility in order to serve an AC load or inject alternating current into the grid.



**Figure I. 6:** PV system with a single phase and a DC-AC converter.

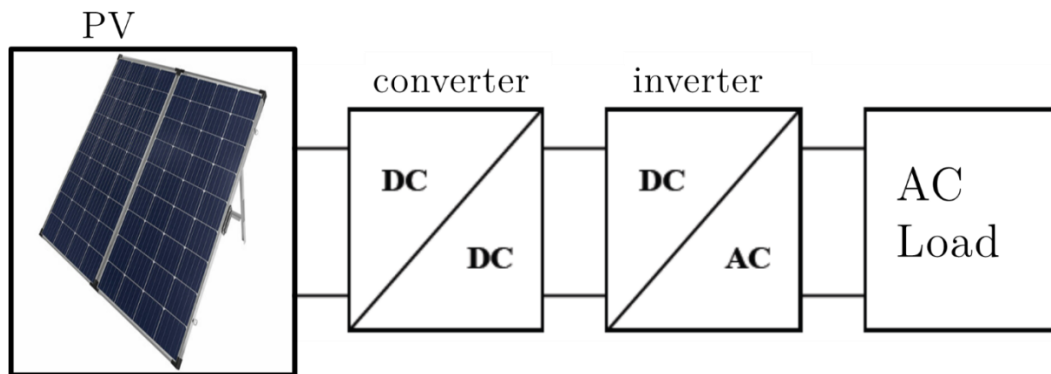
Grid-connected PV systems are often the most employed solution in PV applications, according to statistics in [16]. As a result, converting the DC component from the PV panels

to an AC component becomes mandatory. As a result, several authors have made use of the topology depicted in Figure I.6. A single-stage inverter with voltage boosting capabilities has been suggested by Jain et al. and Caceres et al [17]. The recommended method performs well in terms of conversion quality and current flow into the grid.

Furthermore, Kim et al. employed the standard inverter design to inject a low THD (Total harmonic distortion) current into the grid [18]. The majority of the documented research on single-phase inverters suggest that this topology demonstrates simplicity and reasonable current control [19]. This arrangement, however, suffers from a low range DC voltage, which decreases power quality. As a result, the usage of a dual-stage is advised.

### 3.2. Dual-Stage: DC -AC converters

High efficiency and good conversion quality are required to achieve a high level of accuracy in photovoltaic utilization. As previously stated in the preceding sections, a single-stage conversion cannot meet both criteria in all power ranges. As a result, the two-stage structure shown in figure 1.7 is used. This latter comprises two conversion stages: a DC-DC converter and an inverter. This topology varies depending on the power rating [16].



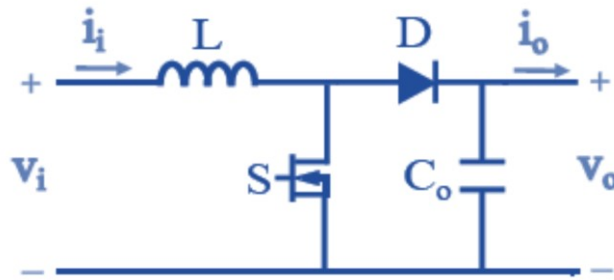
**Figure I. 7:** PV system with a single phase and two stages.

Transferring a controlled voltage to the inverter's input necessitates the usage of DC-to-DC converters. As shown in figure I.7, this design is widely employed in a variety of applications such as pumping systems and energy storage. Diverse types of DC-DC converters are used between the PV module and the load to ensure these functionalities. The key benefits of these converters are their low-cost, high-energy flow, and ability to keep the output constant regardless of input fluctuations. Many types of DC-DC converters have been presented for various uses in the literature.

## 4. DC -DC CONVERTERS

### 4.1. Boost Converter

The boost converter (Figure I.8) is a type of DC-DC converter that can provide an output voltage greater than the input voltage. Due to the conservation of energy, the input power of the boost converter must be equal to the output, which means that the current at the boost's output is less than the input current. This sort of converter is frequently utilized in PV applications due to its high efficiency and ease of implementation.



**Figure I. 8:** DC-DC boost converter.

The boost converter design seen in figure 1.8 is the most common. This topology is used in various PV applications. For example, in 2009 El-Jouni [20] utilised a boost converter to raise the PV panel's supplying voltage. A motor-pump group was powered by the higher voltage at the boost output. The acquired findings show that the system performed admirably.

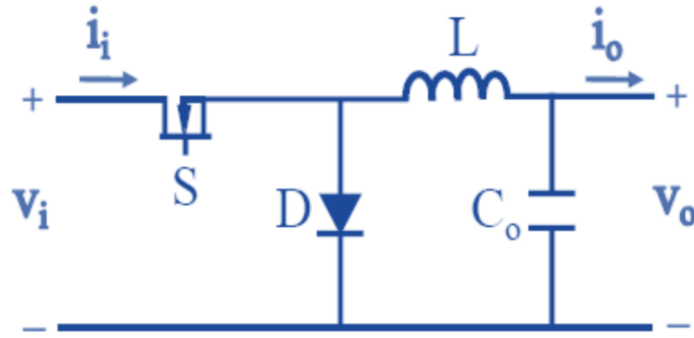
According to Yatimi [21], another role of the boost converter is to supply a DC load, such as a battery. The DC boost converter was used to raise the output voltage to the battery voltage level. Furthermore, other authors modified the conventional topology of figure 1.8 to improve the boost performances. As reported in [22], they proposed an improved version of the traditional boost. This modification is ensured by using a coupled-inductor interleaved to the boost converter. This latter has reduced the switching losses and minimizes the current ripples at the boost converter's input and output.

### 4.2. Buck Converter

The buck converter (Figure I.9) provides an output voltage lower than the input one, contrary to the boost converter. According to the energy conservation law, the buck output current is greater than the input current. In reference [23], the authors designed a four-input buck converter to deliver a controlled voltage to the battery and the DC load. This created configuration provides a cost-effective option by lowering the component count. On the other hand, the authors of [24] employed a buck converter to supply maximum DC power to the



group motor pump. The performance demonstrates that the experimental findings were promising compared to the simulated ones.

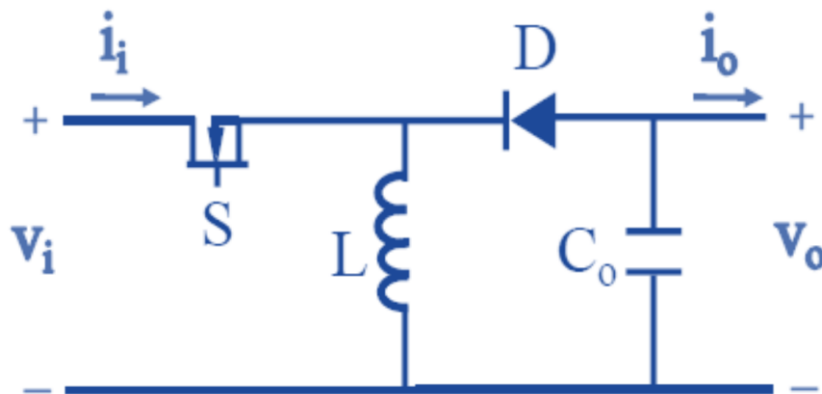


**Figure I. 9:** Buck DC-DC converter.

Several modifications have been made to the traditional structure of figure 1.9 to increase the Buck converter's performance. Hence, the authors of [25] have proposed to vary the input inductance in order to achieve the best system operation based on fluctuations in solar irradiation. Consequently, this topology decreases inductance size by 25% and enables constant output current regardless of solar irradiation fluctuations.

#### 4.3. Buck-Boost Converter

The buck–boost converter is a type of DC-to-DC converter with an output voltage that is either greater than or less than the input voltage (Figure I.10). The fundamental idea behind this latter is to use two control modes by cascading both the boost and buck converters. The advancement of this sort of converter has seen a tremendous increase in the literature over the previous few decades. As a result, many better topologies for buck-boost converters have been created.



**Figure I. 10:** Buck-Boost DC-DC converter.

A buck-boost converter presented in the article of reference [26] proposes a solution using four switches instead of the usual two switches. The results have been verified experimentally and

shown that the proposed topology exhibits high performance and is suitable for some PV applications.

#### 4.4. Other DC-DC Converters

In the literature, other DC-DC converters topologies have been adopted in PV systems according to the area of application. In articles of references [24-26], We have found Cuk, SEPIC, and Zeta converters the most used. The Cuk converter has the same function as the buck-boost converter, but its implementation is complicated.

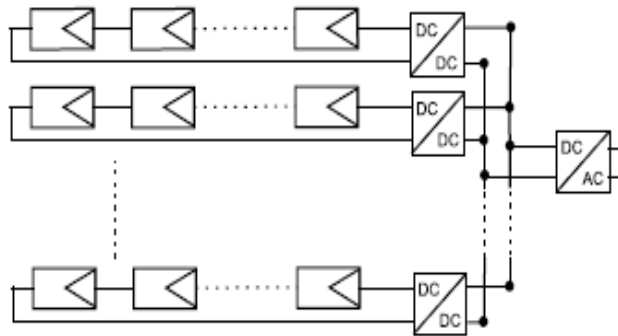
The advantage of this sort of converter is that it provides a constant current at both input and output. In addition, SEPIC and Zeta converters can provide output voltages larger or less than the input voltage. The output voltage of these converters is not reversed, which distinguishes them from buck-boost converters. These types of converters are more extensively utilized in PV applications.

### 5. THE DIFFERENT ARRANGEMENTS OF CHOPPERS IN A PV SYSTEM

In this paragraph, we will present the architectures of PV fields allowing the connection to the distribution network. We are mainly interested in the basic “conversion” function. A great diversity of PV field topologies exists, we will present some of the most used and the most interesting.

#### 5.1. DC/DC converter in parallel row

The use of several conversion stages can improve the conversion efficiency and the reliability of the system, according to [27], by dissociating the functionalities of the inverter (Figure I.11).



**Figure I. 11:** DC/DC converter in parallel row

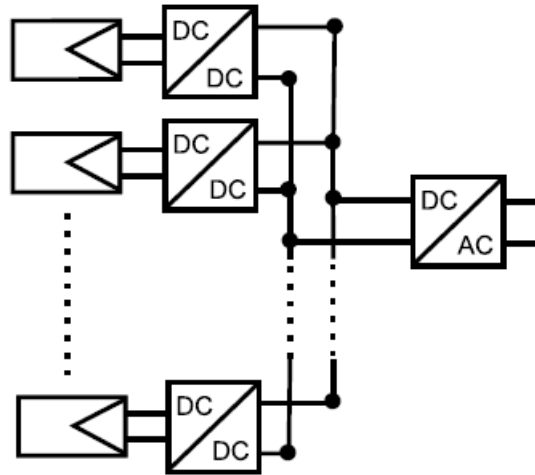
The DC bus has the advantage of quickly incorporating a storage element. In addition, the use of a single inverter as an interface with the grid reduces the number of interactions between

the grid and the PV installation. The MPPT is done for each string, limiting the influence of the modules [28].

The assembly remains scalable, but the continuity of service is not ensured in the event of failure of the inverter [28] and [29].

### 5.2. The modular DC/DC converter in a parallel row

An evolution of the “row” chopper topology is the parallel modular chopper topology shown in Figures 1.12. The chopper is no longer connected to a chain of PV modules but directly to the output of the PV module. Thus, it is no longer a chain of PV modules that operates at its MPPT but each PV module. A gain in productivity is, therefore, to be expected compared to the “row” chopper. In addition, this greater discretization allows finer monitoring and faster fault detection.

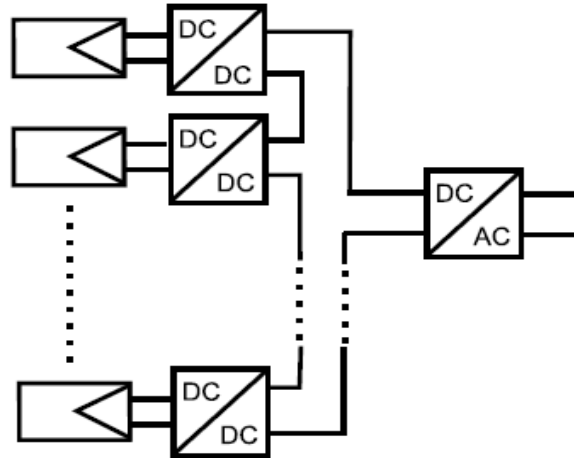


**Figure I. 12:** Modular DC/DC converter in a parallel row

The main hard point of this structure is the large elevation ratio between the output voltage of the PV module and the voltage required for injection into the distribution network. Indeed, for a non-isolated chopper, the higher the elevation ratio, the greater the losses. When this ratio is too high ( $>8$  in general), it is necessary to use isolated structures or cascades of converters. In the present case, the ratio of elevation required is close to 10, limiting the chopper's efficiency and penalising this topology.

### 5.3. The modular DC/DC converter in series row

One of the solutions to reduce the elevation ratio of the choppers necessary for the parallel modular chopper topology is to put the output of the choppers in series. Thus, the elevation ratio is reduced as the number of choppers in series increases. This topology, referred to as the modular serial chopper, is shown in Figure 1-13.



**Figure I. 13:** modular DC/DC converter in series row

This topology retains all the advantages of the previous topology while decreasing the chopper elevation ratio and thus increasing efficiency. On the other hand, the serialization of the choppers implies a dependence of the operating points on each other and complicates the control laws and the dimensioning of the structure.

## 6. INTEGRATION OF PASSIVE COMPONENTS

In recent years, research in electronics has increasingly focused on the integration of passive components in order to achieve a complete integration of power electronics devices cohabiting passive and active components. This integration requires good efficiency, maximum compactness, and good reliability.

Long- and medium-term projects target the reduction of the solar panels size. The miniaturization of converters will perfectly accompany this future's technology. However, the miniaturization of converters requires the integration of its passive components.

To realize compact power converters, several approaches and techniques aim to enhance the capacity of integration of the active and passive components by raising the switching frequency. For example, 3D technology improves the assembly of active and passive components by allowing the simultaneous reduction of modules and interfaces, while lowering connection lengths between components, increasing component's reliability, and saving board and module space [30-32].

### 6.1. The objectives of integrating passive components

To meet the growing needs in power electronics, the integration of passive components must keep pace with active components. The factors listed below help to achieve this goal [33-34].

- Reduce mass, volume, and occupied surface.
- Simplification of cabling by limiting and reducing the number of external interconnections. This favours the reduction of one of the causes of failure and the increase of the reliability of the system.
- Modularity and standardization: Indeed, we note that a certain number of elementary functions are found in each electrical energy conversion system. The objective is to be able to offer elementary bricks, or modules, performing a complete function grouping together several elementary functions, which simply need to be assembled to obtain the desired system. It is necessary that each brick is autonomous and can be connected without problem to the other constituents. The complexity of the circuit is reported inside the modules.
- Greater compactness: Successful integration of passive components is measured not only by the reduction in their own volume, but also by their thermal layout, which can facilitate cooling. Unlike classic passive components that require a heat sink, in integrated component structures overheating phenomena can be mitigated through simplified geometry and a well-studied sizing strategy.
- Increase mass production possibilities.

## **6.2. Integration constraints and limitations**

Although the integration of passive components has the advantages of a minimal volume and performance equal, or better than a discrete solution, many difficult limitations persist and must be overcome; Whether for a monolithic or hybrid integration. The sticking points are almost identical and revolve around the following points:

- The range of use is at low power, which leads to a low energy storage capacity due to the low values of the integrated components.
- The decrease in the size promotes an increase in thermal density, making it more difficult to evacuate heat.
- The incompatibility of the different associated materials in the realization of multilayer structures.
- The manufacturing cost (economic problem): the production techniques are not fully mastered.
- Degradation of the electrical properties of materials for their implementation (curing temperature not compatible with the different used materials) [33].

## **7. BIBLIOGRAPHIC OVERVIEW ON INTEGRATED COILS**

Integrated inductors have been the subject of various scientific studies aimed at better understanding and modelling their electrical behaviour and identifying the different mechanisms at the origin of losses. Several methods of integration of inductive elements can be encountered in the literature. Their objective is to improve the integration density while increasing the inductance value and the quality factor and aiming at operation at ever higher frequencies, with acceptable efficiency.

The concept of miniaturization of the different structures of power electronics is based on the coexistence of different materials: conductive, semi-conductive, magnetic, and dielectric materials. The practical realization calls for mastery of classic microelectronics techniques, such as photolithography, deposition, etching, transfer, interconnection, and assembly technics. These technics have allowed the emergence of many products in different fields of application [33]-[35]

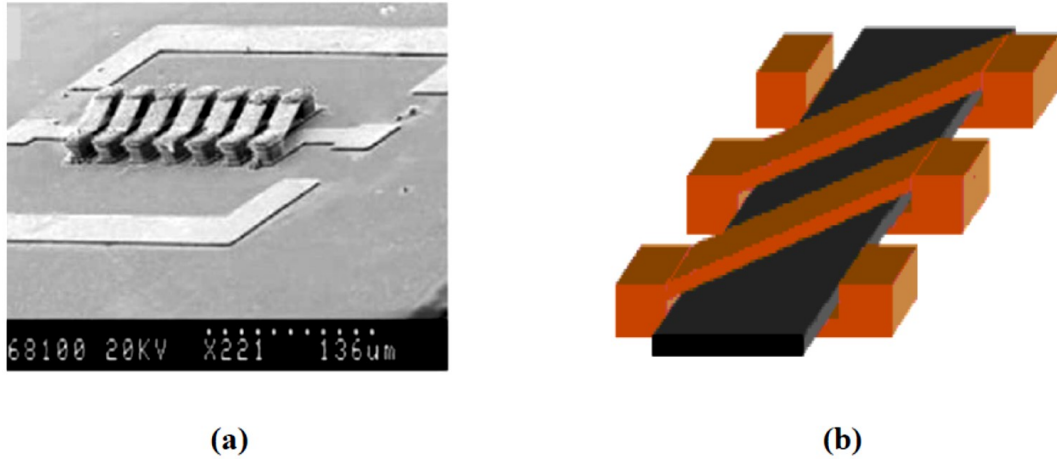
New products are being researched and should soon be industrialized, such as micro-converters. This area is the subject of significant challenges and is currently in perpetual evolution, both in reducing the size of components or the amount of energy to be transferred. However, severe technological hurdles remain to be overcome to make these micro-energy sources compatible with applications presenting tiny sizes and sometimes having to operate in challenging environments. Thus, to be able to design the new power supplies of the future, it is essential, first to design the new passive components of the future, such as inductors, capacitors, transformers.

### **7.1. The different structures of integrated inductors**

In this part devoted to the bibliographic study, we present the evolution of work on integrated inductors with and without magnetic material.

#### **7.1.1. The solenoid structures**

The realization of the solenoidal integrated inductors was inspired by par C.H. Ahn in 1996 from the classic shape of the coils. This inductance type is achieved by stacking three conductive layers (usually copper). In the case of a core-free inductor, the lower and upper layers are separated by an insulating layer. In the case of a ferromagnetic inductor, they are separated by a magnetic layer. The intermediate layer is used to make the vias which connect the two layers, as shown in figure I.14.

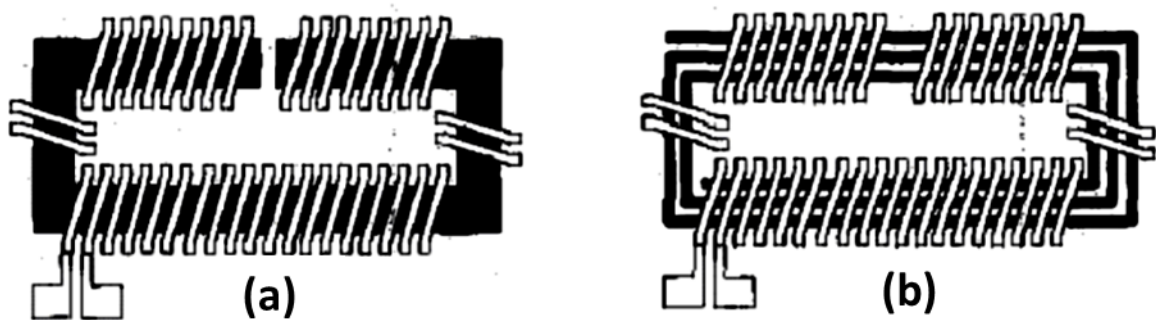


**Figure I. 14:** Integrated coil with solenoid structure, (a) Without core, (b) With magnetic core [35]

In the solenoid structure, the inductance value drops with the rise in frequency, which makes the use of this structure in DC-DC converters of little interest beyond the MHz [35].

To reduce the skin effects and stabilize the effective permeability of the magnetic core, TM Liakopoulos and CH Ahn [41], in later works, proposed two structures deduced from the basic solenoidal structure, one with a localized air gap (Figure I.15 (a)) and the other exhibiting a spiral-shaped laminated magnetic core (Figure I.15 (b)).

The air gap in the two structures stabilizes in frequency the effective permeability of the magnetic core. Despite this, the problem of the differences in expansion of the materials at high temperature intervenes as a defect in these structures.

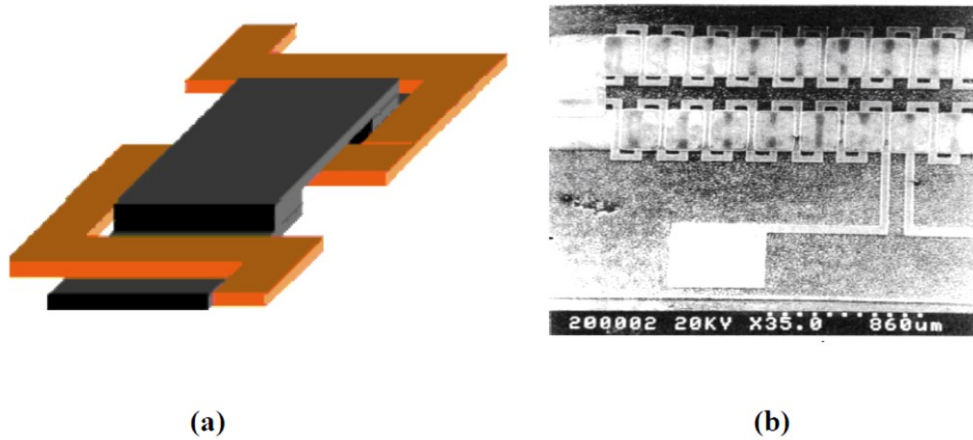


**Figure I. 15:** Solenoid structure, (a) With localized air gap, (b) With laminated core [36]

### 7.1.2. The serpentine structure

Changes have been made to the solenoid structure by removing the intermediate step of realization of the vias between the two levels of conductors and interchanging the geometric

shapes of the magnetic and conductive materials. In this structure, the monolayer conductors set up in the shape of a coil, while the magnetic core is distributed on three levels to wrap the conductor (Figure I.16).



**Figure I. 16 :** Serpentine type coil. (a) Principle, (b) Microscopic view [37]

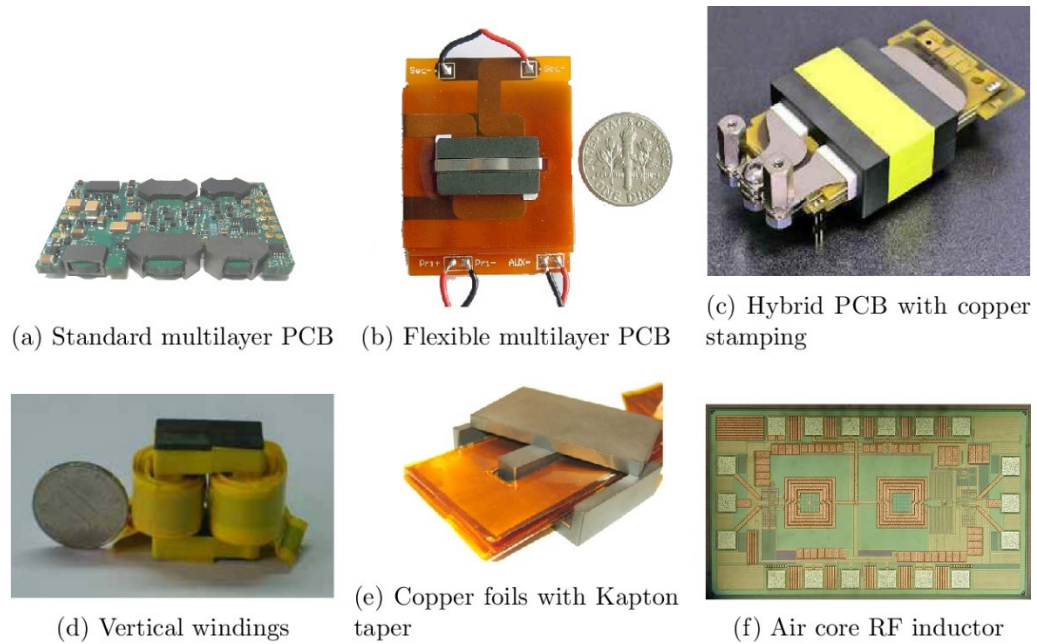
The defect of the serpentine structure is the average length of the core which is greater, which has the effect of increasing the reluctance of the magnetic circuit and thus, reducing the value of the inductance. [37-39].

### 7.1.3. The planar structure

The push toward high-power density, high operating frequency, and low profile in power converters has revealed further research in the integration of magnetic components. The Planar magnetics has become increasingly popular in high-frequency power converters in recent years due to the unique advantages they achieve in terms of low profile, excellent thermal characteristic, good modularity, an easy manufacturing, and the integration on PCB (print circuit board) [39-40].

As illustrated in Fig I.17, there are several approaches for constructing planar windings. Planar structures are often made by laminating planar copper windings and disklike dielectrics onto multilayer PCBs encased in a flat magnetically permeable core. The cost of producing integrated planar magnetics in a PCB assembled power converter has significantly decreased by using flexible foil PCB (FPCB) to construct the windings without increasing the remaining stiff PCB layers [2.1]. Thicker printed copper turns are often utilized in planar construction to accommodate a large current.



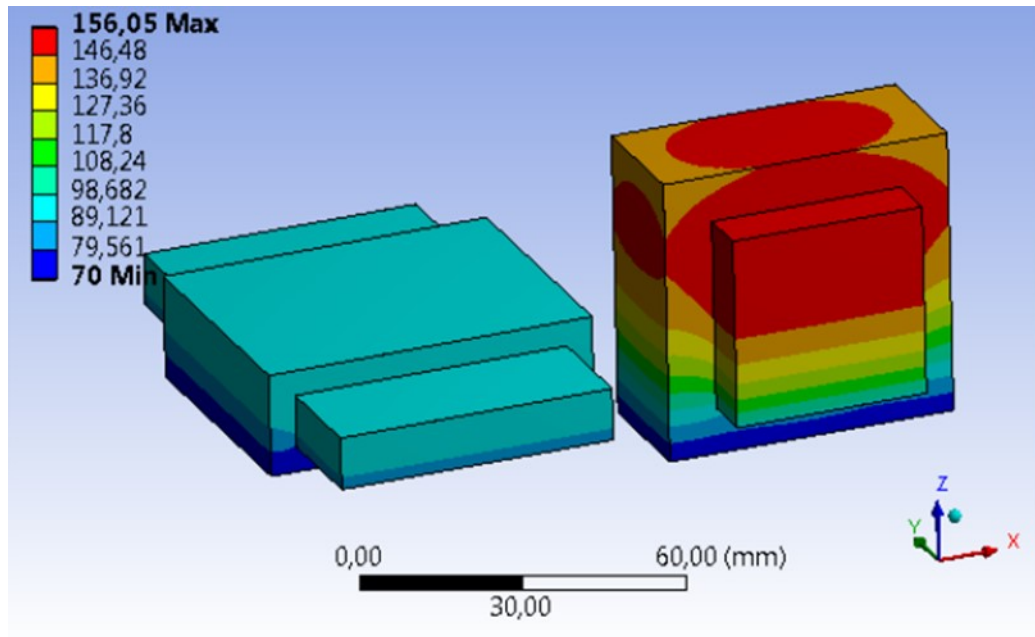


**Figure I. 17 :** Different techniques for implementation of planar windings [41]

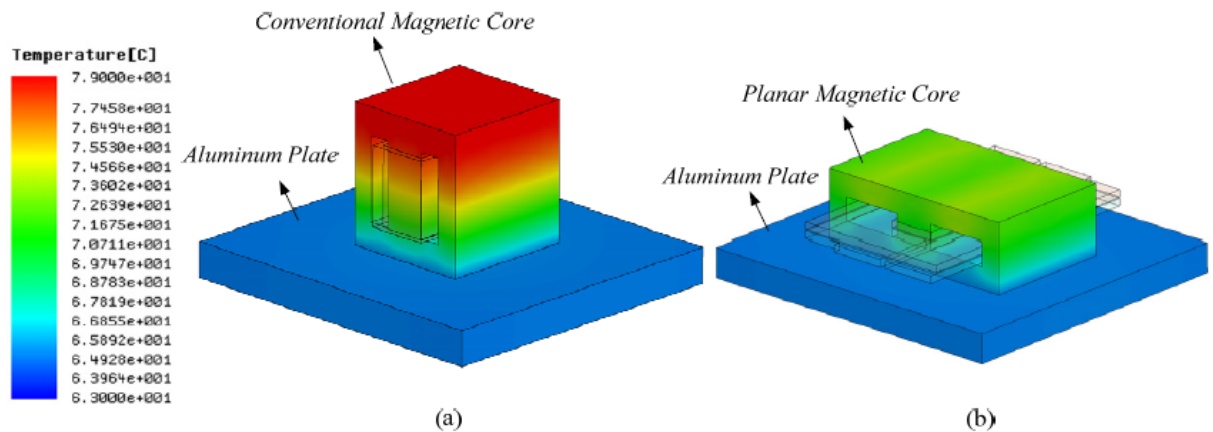
#### 7.1.3.1. Advantages and Disadvantages of the planar structure

The following are the advantages of planar magnetic components compared to traditional components:

- **Low profile:** planar magnetic devices have a substantially lower profile than conventional devices, which helps with shrinking. A planar magnetic device is typically 25% to 50% shorter in height than its equivalent.
- **Good thermal properties and high-power density:** planar magnetic cores offer a larger surface to volume ratio than traditional magnetic cores. As a result, they are more effective at transmitting heat and have lower thermal sensitivities than typical wirewound devices. Figure I.18 and I.19 shows the thermal comparison between conventional core and planar core. It is obvious that the planar core shows a better thermal behaviour than the conventional core. These heat removal benefits add greatly to the power densities.



**Figure I. 18:** Temperature distribution in planar and conventional transformer [42]



**Figure I.19:**Thermal comparison between (a) Conventional and (b) Planar magnetic core [43]

- Ease of manufacture and cost savings: because manual or complex automated stages, such as winding, are eliminated.
  - Ease of implementation on interleaved winding: since multi-layer PCB allow the interconnection of arbitrary layers, interleaved primary and secondary windings can be implemented much more quickly and easily than in conventional magnetics. This provides a significant reduction in leakage inductance and high-frequency winding losses.
- Of fact, not all of the properties of planar magnetics are favourable. They have various restrictions, including:

- Large footprint: the larger surface area provided by planar devices' flatter cores. However, if the core window width is completely utilised, about one-third of the PCB windings surface will be exposed to the ambient air due to the PCB windings being located horizontally, which also adds to the huge footprint.
- High interwinding capacitance: windings stacked closely provides an increased interwinding capacitance, and PCB windings have intrinsically larger surface area than conventional wire-winding, which further increases the interwinding capacitance.

## 8. CONCLUSION

The different used topologies in PV applications have been presented after a Brief overview regarding photovoltaic energy. Also, the single stages are discussed to show the performances and utility of these topologies for each PV application based on the need of feeding isolated sites with AC energy. According to a bibliographic overview, the second part of this chapter has established the present state-of-the-art integration of passive components in particularly, the inductor for the power converter.

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# Chapter II

Designing and Sizing of the Integrated  
Planar Inductor Model for the DC-DC Boost  
Converter.

## 1. INTRODUCTION

Nowadays, the critical role of the power inductor in the electronic industry drives to a competitive race in order to reach for high-efficiency models with very diminutive sizes. Future converters made up of these components are characterized by their very small size, which allows them to be integrated at the back of the photovoltaic module in a very small space.

Today, the system for converting solar energy into electricity still suffers from a lack of optimization which still makes them too expensive systems with poor performances and too heavy equipment.

In this 2nd chapter, we were interested in the coil of a Boost converter dedicated for Photovoltaic energy. Since the conductor section plays a crucial role in the control of the energy losses in coils, we have devoted the greater part of this chapter to studying the influence of the conductor thickness on different parameters of the coil.

In literature we find several mathematical expressions allowing the calculation of the inductance value according to the different inductor geometrical parameters. By analysing these expressions, we have noticed that the conductor thickness is totally neglected and does not appear in any of these expressions, despite its important role in the control of energy losses.

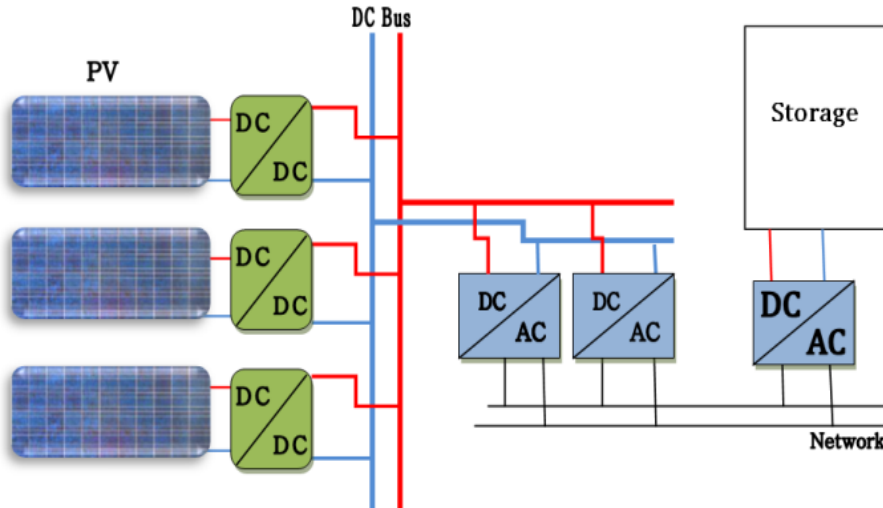
We also find in literature the known condition  $t \leq 2\delta$  or  $w \leq 2\delta$  to circumvent the skin effect which is the source of losses by Joule's effect. If we choose the condition  $t \leq 2\delta$ , what is the optimal value of the thickness "t":  $t \leq 2\delta$  or  $t = 2\delta$ ?

To answer this question, we have conducted an in-depth study to see the influence of the thickness "t" on all parameters contributing to the inductor energy losses. This study allowed us, also, to choose the most optimal condition among these two conditions  $t \leq 2\delta$  or  $t = 2\delta$ .

## 2. PRESENTATION OF THE APPLICATION

The significance of this study rests in its contribution to the conceptual approach for minimizing the size of a DC-DC boost converter. Hence, we have chosen a DC-DC optimizers topology for a photovoltaic system as an application for this research, as shown in figure 01.





**Figure II. 1:** Proposed schematic diagram for electrical connections of a PV system.

The DC optimizers (also known as Module Integrated Converters) in references [1-4], are set up by using a DC-DC converter for each PV module. All these converters are delivering their output voltage in high-voltage DC bus. The physical connection between the DC bus and the utility grid is performed by an inverter as presented in figure 01.

The advantage of this topology, that every single PV module includes its proper MPPT system in the DC-DC converter. It means that the impacts of different shadows, mismatch and a different orientation are totally cancelled [5-8].

The proposed structure allows for easier monitoring of the solar system [9-11], scalability for the PV field, and the replacement of modules. This architecture is more secure than conventional architecture [12-13], because a low-voltage switching is possible at the output of the module, which means the risk of fire is significantly reduced.

The inverter makes it possible to add a redundancy stage and thus reinforce the reliability node which it represented, and in this case, the storage is an optional depending on the installation site and the robustness of the distribution network [13]. In our application the DC bus voltage is set at 220V to allow the inverter to restore the grid voltage. Therefore, it is required to provide a chopper with excellent performance for this architecture, capable of raising the voltage to the needed by the DC bus.

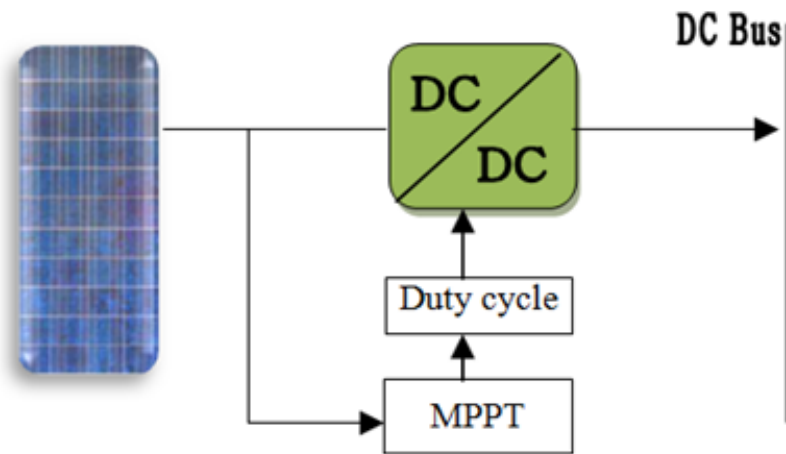
The chopper performs the interface between the output of the PV module and the DC bus. The concept to be created must comply with the present market's crystalline photovoltaic module. The chosen solar panel is made up of 32 cells of a typical silicon polycrystalline solar wafer. Table 1 provides further information about the PV:

	Size	Power (32 cells)
<b>Wafer cell</b>	125mm x 125 mm	17V/5A/85W

**Table II.1:** Nominal inputs of the chopper.

The chopper must be able to handle an input voltage of 0 to 17 volts. 7 A is the maximum input current that must be accommodated. The nominal output voltage is 220V. Overall, the system comprises a PV generator and an MPPT system that sends to the chopper a square wave with a duty cycle  $D$  adjusted according to the voltage delivered by the PV generation. The duty cycle varies depending on the input supplied by the PV panel. This variability allows the output voltage to remain stable.

Figure 2 shows the PV system with MPPT control. Each module connected to the DC bus functioning with its proper duty cycle, which could be different from other modules [14], because the voltage delivered by each module may be different due to the different effects, such as the photovoltaic shading effect or different orientation of angles. The DC bus's stability is better assured in the case of the suggested configuration.



**Figure II. 2:** Diagram of a PV system with MPPT control

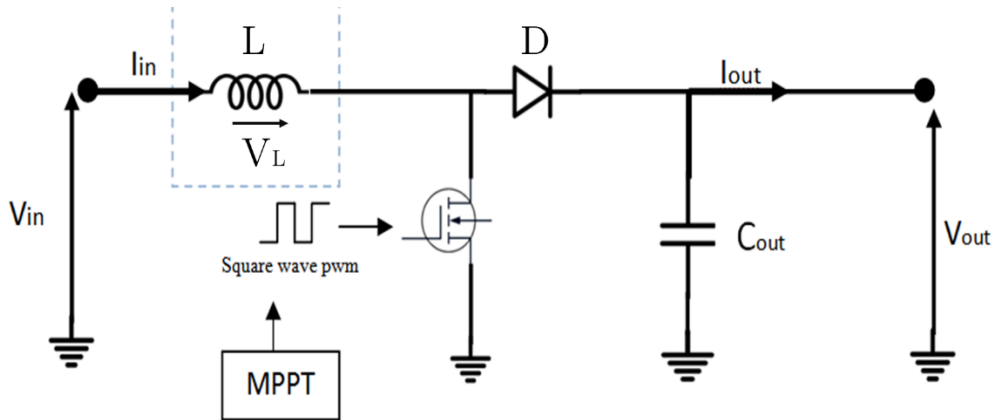
### 3. PRESENTATION OF THE DC-DC POWER CONVERTER

DC / DC converters are used in many applications, with a wide variety of power levels, ranging from less than one watt in converters in small equipment, to ten or a hundred watts in power supplies for desktop computers and photovoltaic systems, to kilowatts or megawatts in the control of variable-speed motors, and up to terawatts in power generation stations [15]. DC / DC converters generally perform two functions: changing the voltage level (raising or

lowering) and regulating the voltage. The conversion electronics are located at the interface between the batteries (the power source in general) and all the system's building blocks under consideration.

In this work, we are focusing our interest on reducing the size of the boost converter for the mentioned application. In general, the passive components (inductors and capacitors) in power converters occupy around 80% of the general volume. Therefore, the size reduction of one or of both components without affecting their performance will certainly reduce the power converter volume and Weight, which is the desired goal. We have picked the inductor of the boost converter shown in figure 3. This converter will be then connected to the PV module.

In this configuration, the DC/DC converter is seated to increase the voltage coming from the photovoltaic module. Figure 03 present the electrical schematic of the suggested boost power converter with a minimum number of switches (one switch) which can work in MPPT mode to produce maximum output at all insolation levels of the solar panel, or it could be used in a similar schematic after this one in order to control the stability of the output supplied to the DC bus.



**Figure II. 3:** Electrical schematic of DC-DC boost converter

#### 4. VALUES OF THE CONVERTER ELECTRICAL PARAMETERS

Since the converter is an intermediary between the energy source and the load, The characteristics of these two elements must be considered during the design to follow and respect the needed specifications during the modelling. Our choice is based on a power boost DC-DC converter that meets the parameters presented in table 2:

Operating frequency $f$	500 KHz
Input voltage $V_{in}$	17 V
Output voltage $V_{out}$	220V
Maximum current of the coil $I_{Lmax}$	$\leq 7A$
Average coil current $I_{Lavg}$	5A
Operating temperature $T$	Till 80°C
Ripple of the output voltage $\Delta V_{out}$	<0.8%
The reserved volume for the inductor	12*12*10 mm <sup>3</sup>

**Table II.2:** Boost DC-DC converter specifications.

#### 4.1. Duty cycle determination

PWM (Pulse Width Modulation) is the control signal for the power switch (MOSFET), dependent of a  $D$  duty cycle.  $D$  is calculated using expressions (II.1) and (II.2).

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \quad \text{Equation (II.1)}$$

$$D = 1 - \frac{V_{in}}{V_{out}} \quad \text{Equation (II.2)}$$

According to equation (II.2), the duty cycle  $D$  is around 92.27 %. We can deduct from the previous equations that the output voltage is related directly to the duty cycle. This shows the possibility of output voltage correcting is always feasible by changing the value of the duty cycle  $D$  .as the solar panels generate varied output throughout the day depending on many factors [16].

#### 4.2. Calculation of inductance value and current ripples values

To determinate the Value of inductance  $L$  we need firstly to calculate the inductor current ripples value  $\Delta I_L$  by using equation (II.3):

$$I_{Lmax} = I_{Lavg} + \frac{\Delta I_L}{2} \quad \text{Equation (II.3)}$$

The inductance  $L$  is calculated from equation (II.4)

$$L = \frac{V_{in} \times D}{f \times \Delta I_L} \quad \text{Equation (II.4)}$$

The calculated inductance value is around 7.84  $\mu\text{H}$ , for an inductor current ripple of 4A calculated from equation (II.4).

Equation 4 shows an inversely proportional relationship between the inductance L and the inductor current ripple  $\Delta I_L$ . So, we decided to increase the inductance L to 10  $\mu\text{H}$  in order to reduce current ripple, and by that, but, the maximum current in the inductor would be less than the mentioned on the specifications tables as required.

### 4.3. Output capacitance value calculation

The target of adding a capacitor in parallel with the load is to reduce the output voltage ripple [17]. This process leads to the charge of the capacitor when the power switch is opened. once, the switch is closed, the capacitor is able to provide energy for the load [18].

The Target of adding a capacitor in parallel with the load is to reduce the output voltage ripple [17]. This process leads to the charge of the capacitor when the power switch is opened. Once the switch is closed, the capacitor is able to provide energy for the load [18].

The  $C_{out}$  output capacitor value, calculated from equation (II.5) is  $40,64 \times 10^{-8}$  F.

$$C_{out} = \frac{I_{out} \times D}{f \times \Delta V_{out}} \quad \text{Equation (II.5)}$$

For better performance on the level of the output voltage and more reducing the ripples, we can increase the output capacitor value to  $50 \times 10^{-8}$  F.

### 4.4. Calculation of the output current and load values

The output current value  $I_o$  and the load  $R_{load}$  value are calculated from equations (II.6) and (II.7.)

$$I_{out} = \frac{I_{in} \times V_{in}}{V_{out}} \quad \text{Equation (II.6)}$$

$$R_{load} = \frac{V_{out}}{i_{out}} \quad \text{Equation (II.7)}$$

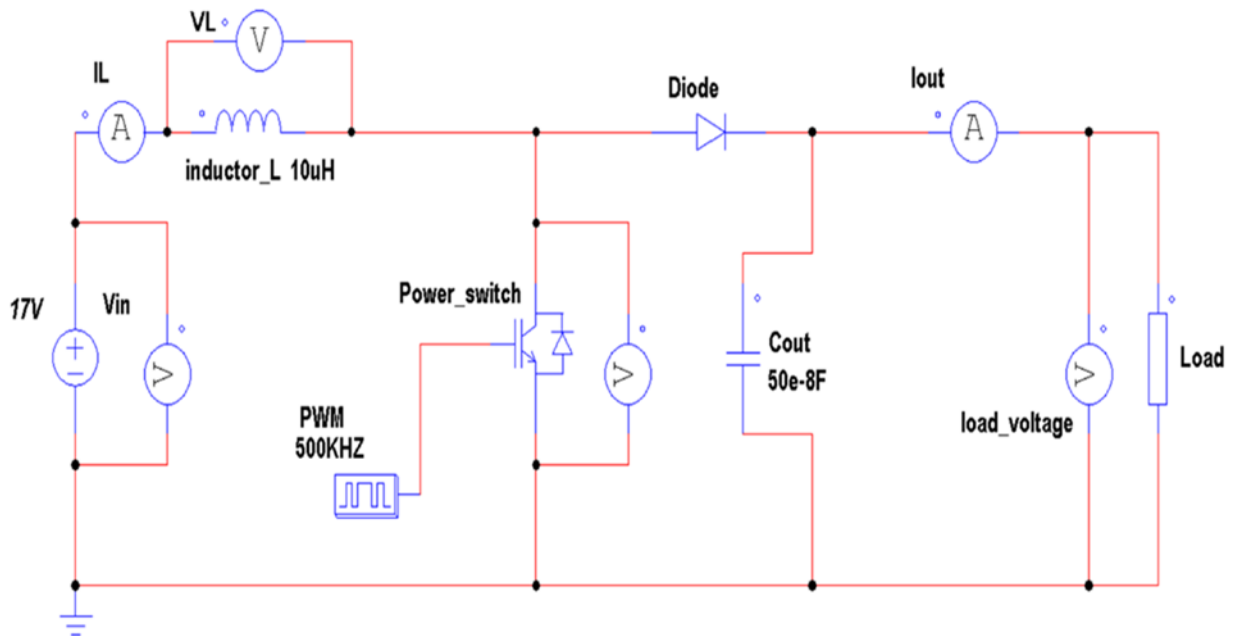
The calculated dc-dc boost power converter parameters are grouped in table II.3:

$V_{in}$	$V_{out}$	D	$\Delta I_L$	$I_{L_{max}}$	$I_{L_{min}}$	$I_{L_{avg}}$
17V	220V	92.28%	4A	7A	3A	5A
L	$C_{out}$	$I_{out}$	$R_{load}$	$\Delta V_{out}$	Frq	
10 $\mu$ H	$50 \times 10^{-8}$ F	0.38A	569.5 $\Omega$	1.76V	500kHz	

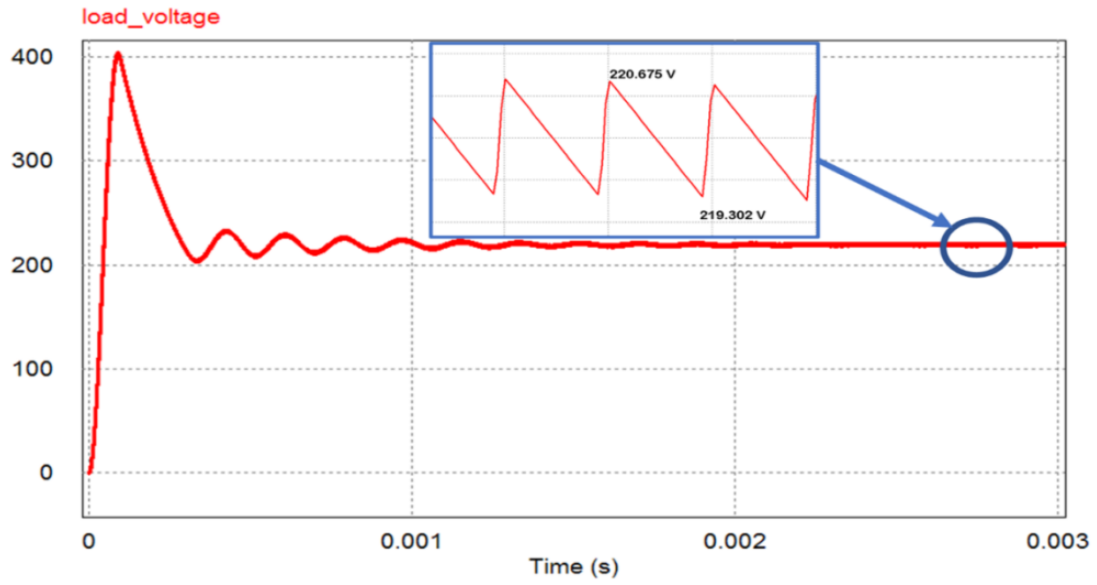
**Table II.3:** The calculated DC-DC boost parameters

#### 4.5. Validation of the good converter operating

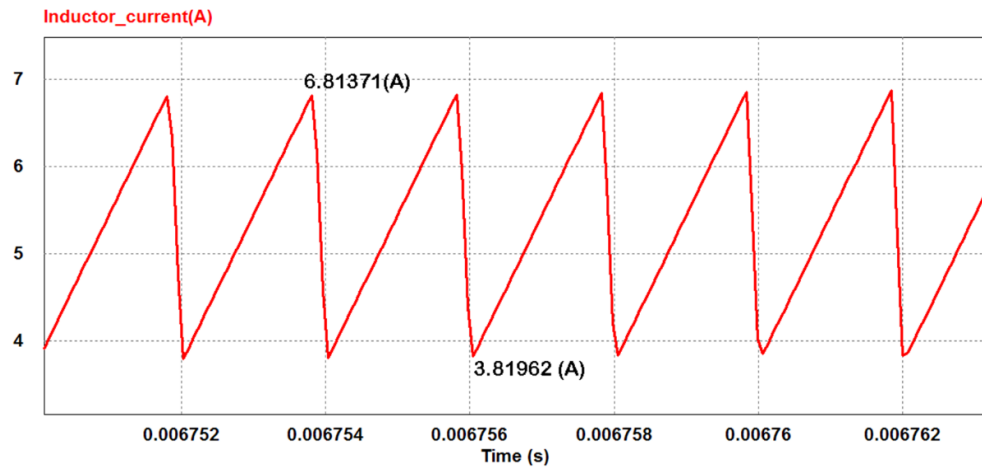
To validate the results obtained in the previous section, as well as the good operating of the DC-DC power boost converter, we used PSIM software to simulate the different waveforms of the output current, the output voltage and the current flowing in the coil (Figure II.3 and II.4). These simulations permit us to ensure that the results obtained respect the conditions schedule in table II.2. They will also serve as references, when the perfect coil in circuit of figure II.4 is replaced by the miniaturized coil.



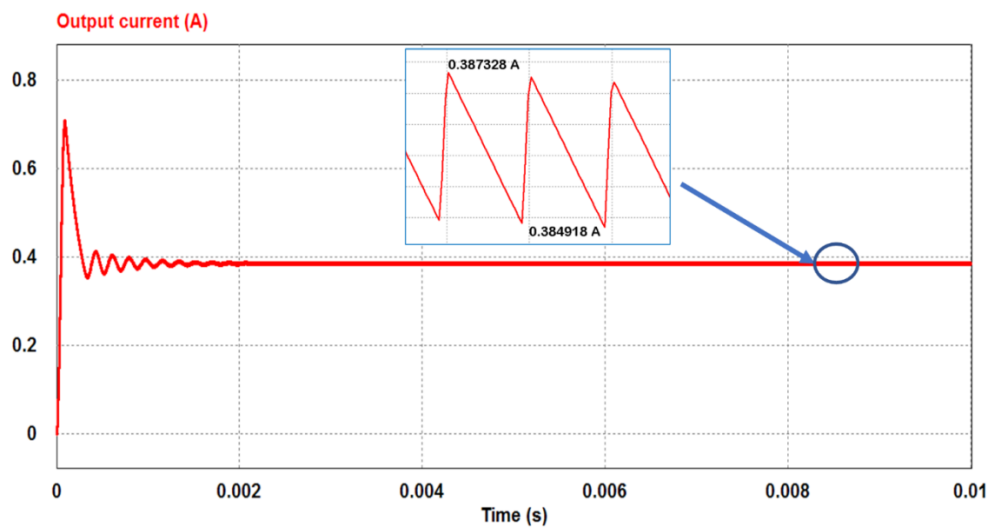
**Figure II. 4:** PSIM schematic of the boost converter



**Figure II. 5:** The DC-DC boost converter output voltage waveform



**Figure II. 6:** The inductor current waveform



**Figure II. 7:** The DC-DC boost converter output current waveform

Figure II.5-II.6 and II.7 shows satisfactory results. All conditions in schedule of conditions are respected and the output voltage ripple is close to 0.8%V<sub>out</sub>.

## 5. GEOMETRIC DIMENSIONING OF THE COIL AND ITS MAGNETIC CORE.

### 5.1. Choice of the geometry

As mentioned previously, our main objectify is to get at the end of this research an optimized volume for the Boost converter's inductor. After a thorough literature research, planar coils took our attention. Therefore, we build up our strategy due to all the advantages given by such a type of technology, where the planar components are promising for use in rack-mount and versatile hardware. Additionally, it characterized by low leakage inductance and high-density power throughput. The planar coils are described by five geometric parameters: the internal and external diameters " $d_{in}$  and  $d_{out}$ ", the width and the thickness of the conductor " $w$  and  $t$ " and the distance between turns " $s$ ".

To determine the coil inductance value, there are several methods based on the geometric form for the planar coils. The analytic expression (II.8) presented by Monomial [18] takes into account the conductor width  $w$ , the average diameter  $d_{out}$ , the number of turns  $n$  and also the space inter-spires  $s$ .

$$L = \beta d_{out}^{\alpha1} W^{\alpha2} d_{avg}^{\alpha3} . n^{\alpha4} S^{\alpha5} \quad \text{Equation (II.8)}$$

The values of the coefficients presented in Table II.1 depend on the geometric form of the spiral coil.

Geometry	$\beta$	$\alpha1$	$\alpha2$	$\alpha3$	$\alpha4$	$\alpha5$
<b>Square</b>	1.62e-3	-1.21	-0.147	2.4	1.78	-0.03
<b>octagonal</b>	1.28e-3	-1.28	-0.174	2.47	1.77	-0.049
<b>hexagonal</b>	1.33e-3	-1.21	-0.163	2.43	1.75	-0.049

**Table II.4:** The coefficients of Monomial formula

For the case of Bryan's method [20,21] the formula is based on the external diameter  $d_{out}$ , the number of turns  $n$ , and the average diameter  $d_{avg}$  (Expression II.14) and the form's factor  $\rho$  (Expression II.13) as it's shown in expression (II.9):



$$L = 0.024 \frac{d_{avg}}{2} n^{5/3} \ln\left(\frac{4}{\rho}\right) \quad \text{Equation (II.9)}$$

In the method of Terman [22], the expression is determinate by taking into consideration several of geometric parameters ( $d_{in}$ ,  $d_{out}$ ,  $s$ ,  $w$ ) as shown in in expression (II.10):

$$L = \frac{\mu_0 d_{out}^3}{4\pi(w+s)^2} \cdot \left[1 - \left(\frac{d_{in}}{d_{out}}\right)^2\right] \cdot \left(1 - \frac{d_{in}}{d_{out}}\right) \cdot (0.2235\rho + 0.726 - \ln \rho) \quad \text{Equation (II.10)}$$

The formula (II.11) given by Mohan [23] it's depend of the value for the average diameter  $d_{avg}$  and the form's factor  $\rho$ , also number of turn  $n$  and four coefficients ( $C_1, C_2, C_3, C_4$ ), where the value of these coefficients depend on the form of the coil as shown in table II.5:

$$L = \frac{\mu_0 \cdot n^2 \cdot d_{avg} \cdot c_1}{2} \left[ \ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2 \right] \quad \text{Equation (II.11)}$$

Geometry	$c_1$	$c_2$	$c_3$	$c_4$
square	1.27	2.07	0.18	0.13
hexagonal	1.09	2.23	0	0.17
circular	1	2.46	0	0.20
octagonal	1.07	2.29	0	0.19

**Table II. 5:** The coefficients of Mohan

Wheeler also has several expressions for spiral coils [24]. And to obtain more precision in the calculated inductance value. Mohan reached to formulate the equation of shape in expressions (II.12) named "modified Wheeler formula".

$$L = k_1 \mu \frac{n^2 d_{avg}}{1 + k_2 \rho} \quad \text{Equation (II.12)}$$

Where  $k_1, k_2$  are coefficients corresponding to the form geometry, the value of these coefficients are shown in table II.6 , the average diameter  $d_{avg}$  and form factor  $\rho$  are given by the expressions (II.13 and II.14)

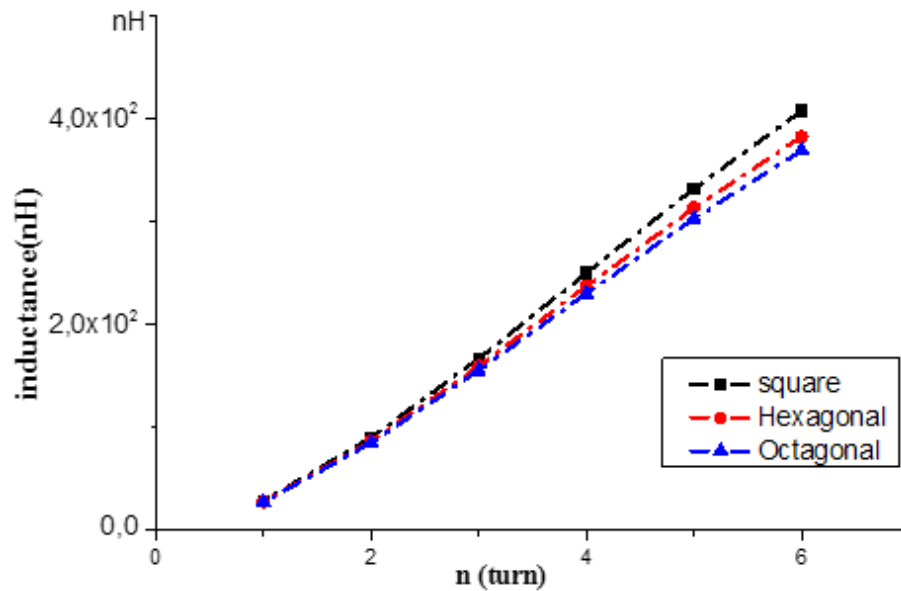
$$\rho = \frac{d_{out} - d_{in}}{d_{out} - d_{in}} \quad \text{Equation (II.13)}$$

$$d_{avg} = \frac{(d_{out} - d_{in})}{2} \quad \text{Equation (II.14)}$$

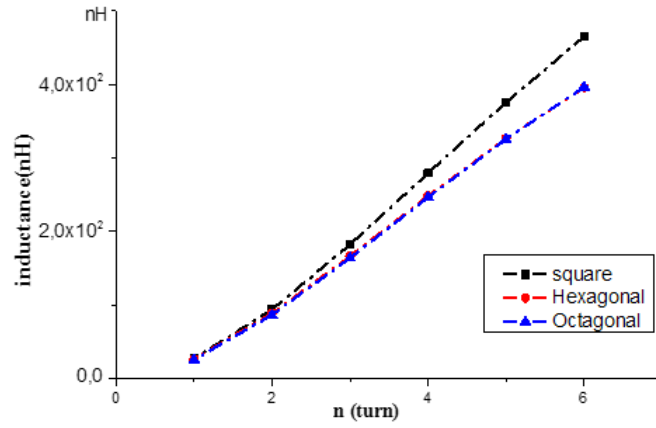
geometry	$k_1$	$k_2$
square	2.34	2.75
hexagonal	2.33	3.82
octagonal	2.25	3.55

**Table II. 6:** The modified coefficients of Wheeler formula

A spiral planar square inductor was selected, after comparing the behaviour of inductors with different geometrical shapes, by using the modified Wheeler formula (II.12) and Monomial formula (II.8). By taking into consideration of the same geometric parameters for different forms. The graph in Figures (II.8 and II.9) shows that the inductance for square coil keeps the highest value, compared with other forms using two different formulas. Following these comparison results, we opt for the square spiral inductor because, the main purpose is to have the highest inductance value for the smaller size possible.



**Figure II. 8:** Different inductance curves using Monomial formula



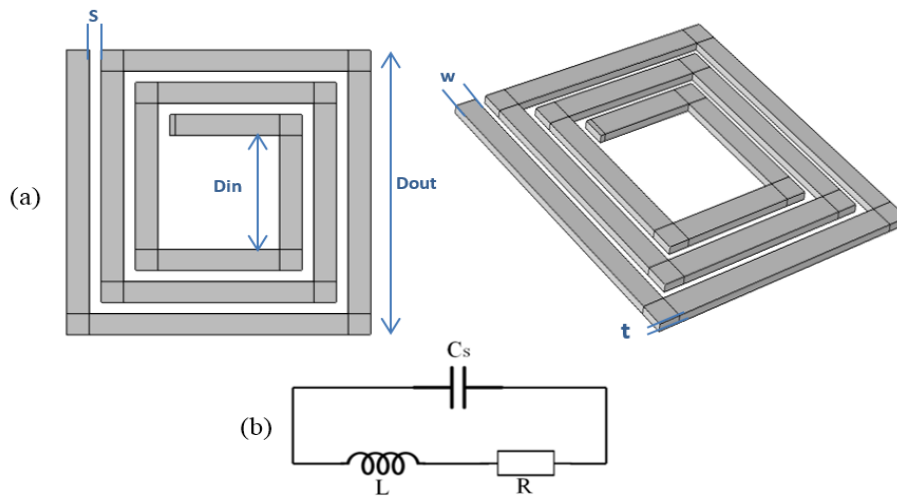
**Figure II. 9:** Different inductance curves using Wheeler formula

## 6. SINGLE LAYER SQUARE SPIRAL PLANAR INDUCTOR

The maximum space reserved for the inductor on the boost converter's electronic board should not exceed 12mm x 12mm x 10mm. This condition will be considered during the geometrical dimensioning of the inductor presented in Figure II.10 (a). Its electrical equivalent circuit is represented in Figure II.10 (b). Where  $L$  is the inductance,  $R_s$  and  $C_s$  are respectively, the conductor's self-resistance calculated from equation II.15 and the total capacitor created between the coil turns expressed by equation II.16.

$$R_s = \rho \frac{l_{moy}}{w t} \quad \text{Equation (II.15)}$$

$$C_s = \epsilon_0 \cdot \frac{t \cdot l_{active}}{s} \quad \text{Equation (II.16)}$$



**Figure II. 10:** The chosen coil geometry (a) 3D modelling for the chosen coil geometry (b) The electrical equivalent schematic

The parasitic elements: resistance  $R_s$  and the capacitor  $C_s$  both affect the inductance value  $L$ . Therefore, it can be concluded that the inductance  $L$  depends strongly on the conductor thickness  $t$ . It's also noticeable that the conductor thickness  $t$  is inversely proportional to  $R_s$  and at the same time proportional to  $C_s$ . which makes the choice of the thickness  $t$  difficult.

### 6.1. Influence of the conductor thickness on the inductance value

All different formulas mentioned in paragraph 5.1, allow to determine an approximate value of the coil's inductance. In each expression, the inductance  $L$  is calculated according to the geometrical parameters;  $n$ ,  $D_{out}$ ,  $d_{in}$ ,  $s$ , and  $w$ . But we noticed that none of these expressions includes the conductor thickness  $t$ , although the thickness  $t$  has an important impact on the inductance value. As mentioned before, the thickness  $t$  is proportional to the parasitic capacitance  $C_s$ , which mean when  $C_s$  is large, it degrades the inductor's performance due to the leaked current between turns.

In order to see the direct impact of the conductor thickness  $t$  on the inductance value  $L$ , we will use the COMSOL simulation software and the data of our dimensioned planar coil in order to extract an expression allowing to calculate the inductance value  $L$  according to the thickness " $t$ ".

#### 6.1.1 Predesigning of the single-layer square spiral planar inductor

The maximum section recommended for the inductor is 12mm x 12mm. We suggest as predesigning of the inductor: an external diameter  $D_{out}=10\text{mm}$ , an internal diameter  $d_{in}=4\text{mm}$ , conductor's width  $w=470$  and a number of turns  $n=3$  respecting the condition mentioned in table II.2, then, we calculate the inter-turns distance  $s$  by using expression II.17. All values of the geometrical parameters are grouped in Table II.7.

$$s = \frac{D_{out} - d_{in} - 2wn}{2(n-1)} \quad \text{Equation (II.17)}$$

$D_{out}$	$d_{in}$	$s$	$w$
10 mm	4 mm	390 $\mu\text{m}$	470 $\mu\text{m}$

**Table II. 7:** Single layer inductor parameters

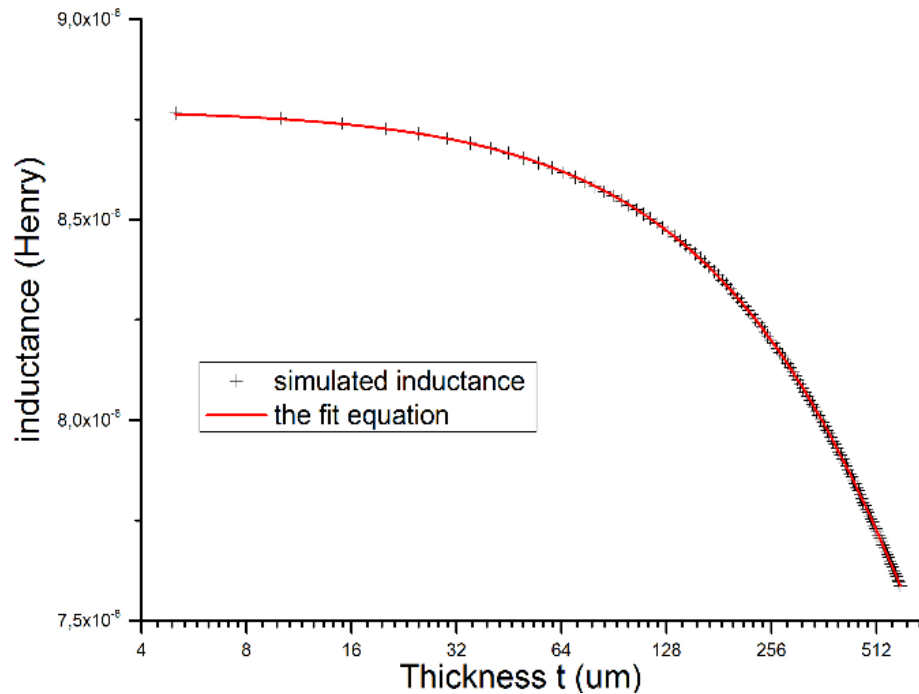
### 6.1.2. Influence of the conductor thickness

As we mentioned previously, none of the methods presented in the literature takes into consideration the conductor thickness in the calculation of the inductance  $L$ . To introduce this parameter, a numerical simulation by COMSOL Multiphysics was done for the geometry presented in figure II.10 taking into account the results of Table II.7.

By varying the thickness value " $t$ " from 5  $\mu\text{m}$  to 600  $\mu\text{m}$ , we obtain an inductance value  $L$  for each thickness  $t$ . the different values of the inductance  $L$  obtained by simulation represent the ordinates of the black points in figure II.11. Simulation results are obtained by solving Maxwell's equations ( $\nabla \vec{J} = 0$ ,  $\nabla \times \vec{A} = \vec{B}$ ,  $\nabla \times \vec{H} = \vec{J}$ ,  $\vec{E} = -\nabla V$ ,  $\vec{J} = \sigma \vec{E}$ ) that remain valid in all settings investigated. As a result, we will only discuss the physical models and boundary conditions that are the same for each different  $t$ .

Following the analysis of the results, equation II.18 is formulated to characterise the inductance behaviour according to the conductor thickness. Where  $L$  is the inductance,  $t$  is the conductor thickness,  $P_1$ ,  $P_2$ ,  $P_3$ ,  $P_4$  are the coefficients presented in table II.8.

Expression II.18 is graphically represented by the red curve in figure II.11. It fits 97% of the simulated results.



**Figure II. 11:** Variation of the inductance according to the conductor thickness

$$L = \left( P_1 \times e^{\left( \frac{-t}{P_2} \right)} \right) + P_3 + (P_4^t) \quad \text{Equation (II.18)}$$

$P_1$	$P_2$	$P_3$	$P_4$
3,82249E-7	4758,70836	-2,94489E-7	5,56531E-11

**Table II. 8:** Coefficients values

## 6.2. Selection of the optimal conductor thickness

The choice of the optimal thickness  $t$  allows keeping the size conductor within the permitted range without causing problems like overheating from skin effect or a lack of power from high losses. according for all of that we have done numerical investigation in order to opt the proper thickness.

It's known that when an alternating current flows through a conductor, it is not distributed uniformly throughout the conductor section. AC current tends to circulate at the periphery of the conductor on a thickness  $\delta$  called "skin thickness" and expressed by formula (II.19)

Also, when two or more alternating current conductors are close to each other cause the proximity effect, the current distribution in each conductor is modified by the varying magnetic field of the other conductor. The alternating current's fluctuating magnetic field causes eddy currents in the nearby conductors. As a result, when the currents flowing through the close conductors are in the same direction, a direct proximity effect appears and the current is concentrated at the conductors distant side, when these currents are in opposite directions, the proximity effect is indirect and the current is concentrated at the conductors' closest points.

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi \mu f}} \quad \text{Equation (II.19)}$$

With  $\rho_{cu} = 1.7e-18 \Omega.m$ ,  $\mu_r = 1$  H/m  $\mu_0 = 4\pi 10^{-7}$ ,  $\mu = \mu_r \cdot \mu_0$

For an Operating frequency  $f=500\text{Khz}$ , the calculated skin thickness is  $\delta = 92.84 \mu m$ .

In literature, we generally apply one of both conditions  $w \leq 2\delta$  or  $t \leq 2\delta$  to avoid unused volume of the conductor, and allow the current to pass through its entire section. It should be noted that the more the thickness or the width of the conductor decreases, the more the current density increases and leads to greater Joule losses and heating of the conductor. For these reasons, we will study two different cases:  $t < 2\delta$  and  $t = 2\delta$ . Depending on the obtained results,

we opt for the optimal thickness in order to have the minimum size without affecting the inductor's performance, especially as the application runs with an important current.

As mentioned before, too low conductor thicknesses cause the current density increase and rise the AC resistor of the inductor; the opposite causes a drop in the inductor's inductance and increases its volume. In this part, we used the numerical simulation to understand the behaviour of some important parameters related to the conductor thickness and affecting the operation of the inductor, such as, quality factor, AC resistance, AC losses. inductance, magnetic field and the current density of the inductor.”

### 6.2.1. Magnetic flux simulation for different conductor thicknesses

The numerical simulation was done to observe the magnetic flux and current density for three samples of different thicknesses  $t$ :  $[60\mu\text{m}, 185\mu\text{m}, \text{ and } 360\mu\text{m}]$ . The same initial condition was applied to solve the problem by the finite element method. The numerical results are presented in figures II.12 and II.13.

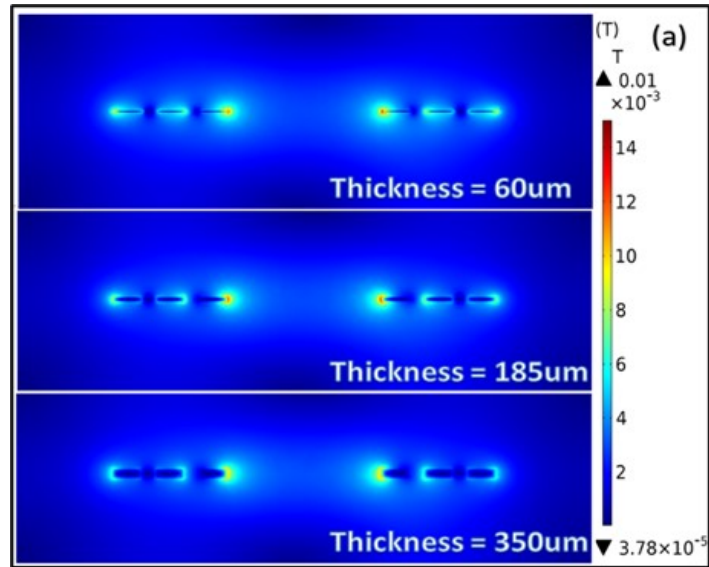
Figure II.12 and II.13 present for different conductor sections, (a) the magnetic flux in conductors, (b) the variation of the magnetic flux density norm along the arc length presented in (c), as well as current density and magnetic field lines in (d).

By analysing the results obtained in figures II.12 and II.13, we note that the magnetic flux is much more intense for the smallest sections and degrades as the sections increase (a). The variations of this flux are presented by curves of figure (b). The three curves are almost superimposed, except for the peaks which differ. We notice more significant rise for the magnetic flux density in the most tiny thickness compared to the others, it is obviously due to the different current densities.

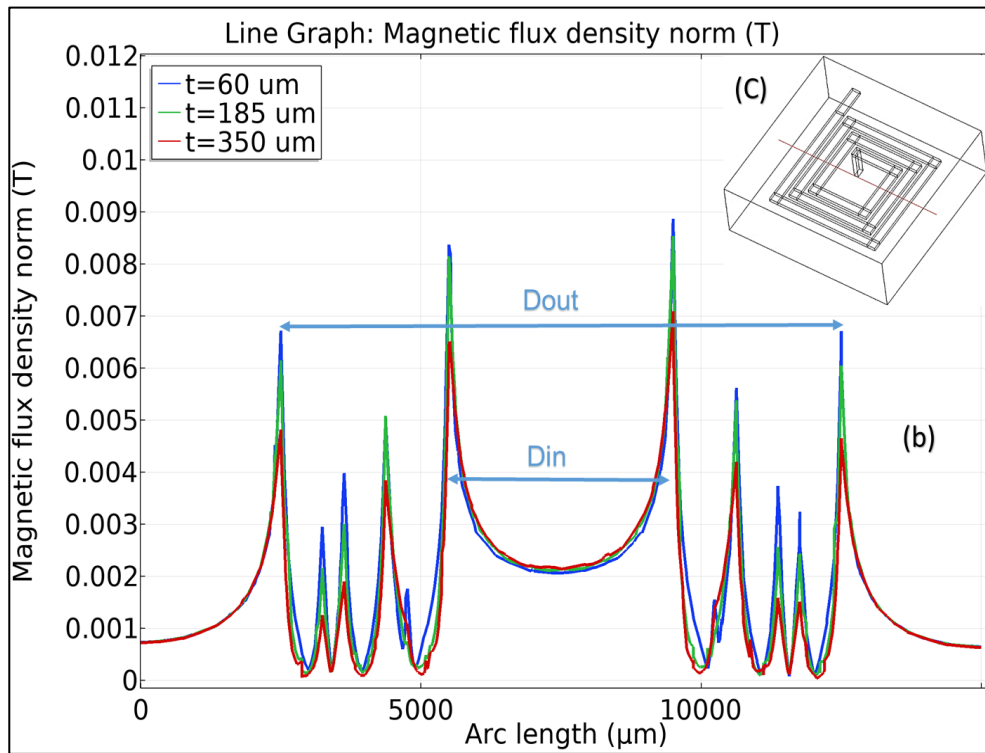
For the thickness  $t=60\mu\text{m}$ , it's noted a very high magnetic flux density in the interior conductors facing internal diameter. This flux concentration may present a danger of a substantial increase in temperature resulting in the failure of the inductor. That makes this option unlikely. For a thickness  $t=180\mu\text{m}$ , the values of the magnetic flux peaks are slightly lower compared to the previous case and lower when  $t=360\mu\text{m}$  (Figure II.12 (a)).

The obtained results do not allow to decide for the optimal thickness of the conductor, because other parameters need to be compared, such as: the current density, the energy losses, etc.

Whereas in these two cases it seems that there is a better distribution comparing to the previous one, and since that the inner region is wider than the previous one, that contributes to reducing the accumulation of magnetic flux in a tiny area (Figure II.12 (b)).



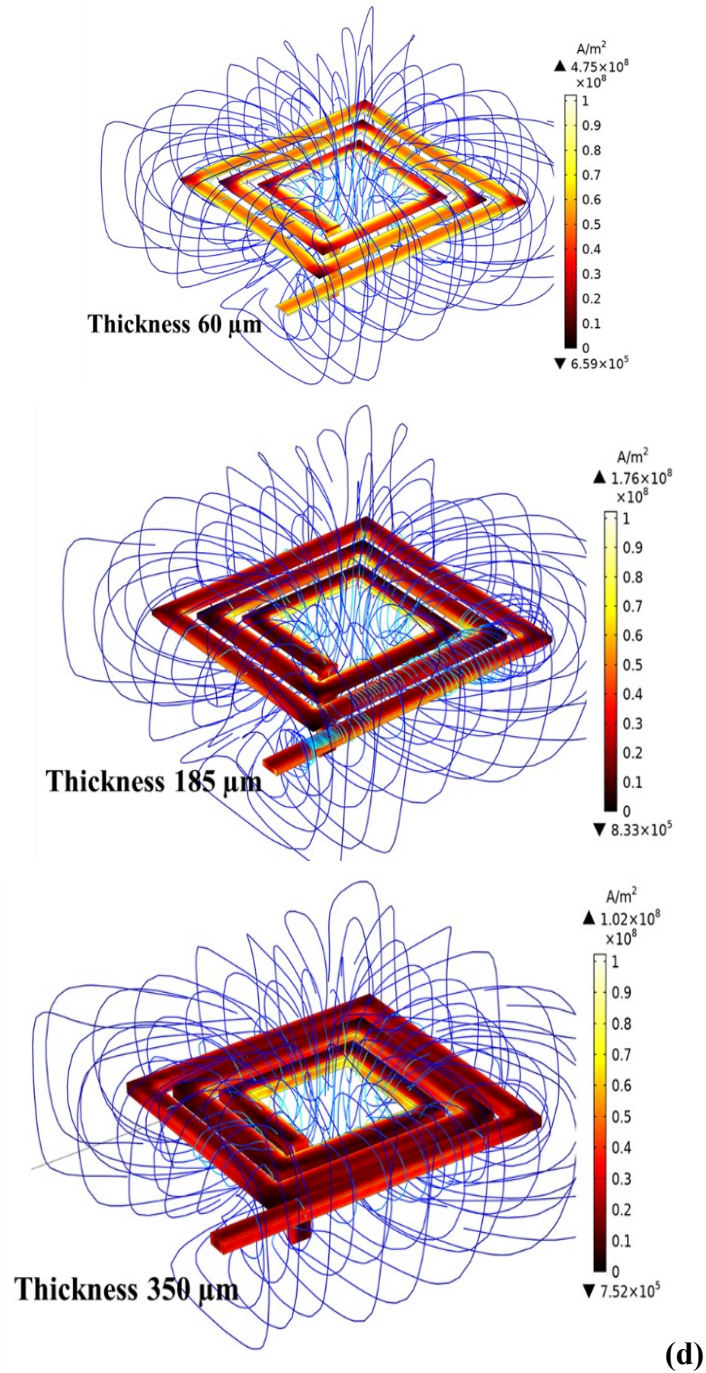
(a): 2D cross section shows the magnetic flux density



(b): Cross-sectional plot magnetic flux density along the arc length mentioned in (c)

**Figure II. 12:** Simulation of magnetic flux density





(d): 3D view for the current density and magnetic flux streamlines for each case.

**Figure II. 13:** Simulation of electromagnetic effects

### 6.2.2. Current density simulation for different conductor thicknesses

To well control the distribution of the electrical current density in conductor; it's necessary to take into account the controlling factors, such as: The applied frequency, which is the leading cause for the phenomenon of Skin Effect in conductors [25-26] and the direction of the electric current in juxtaposed conductors. It can generate a direct or inverse proximity effect [27-28].

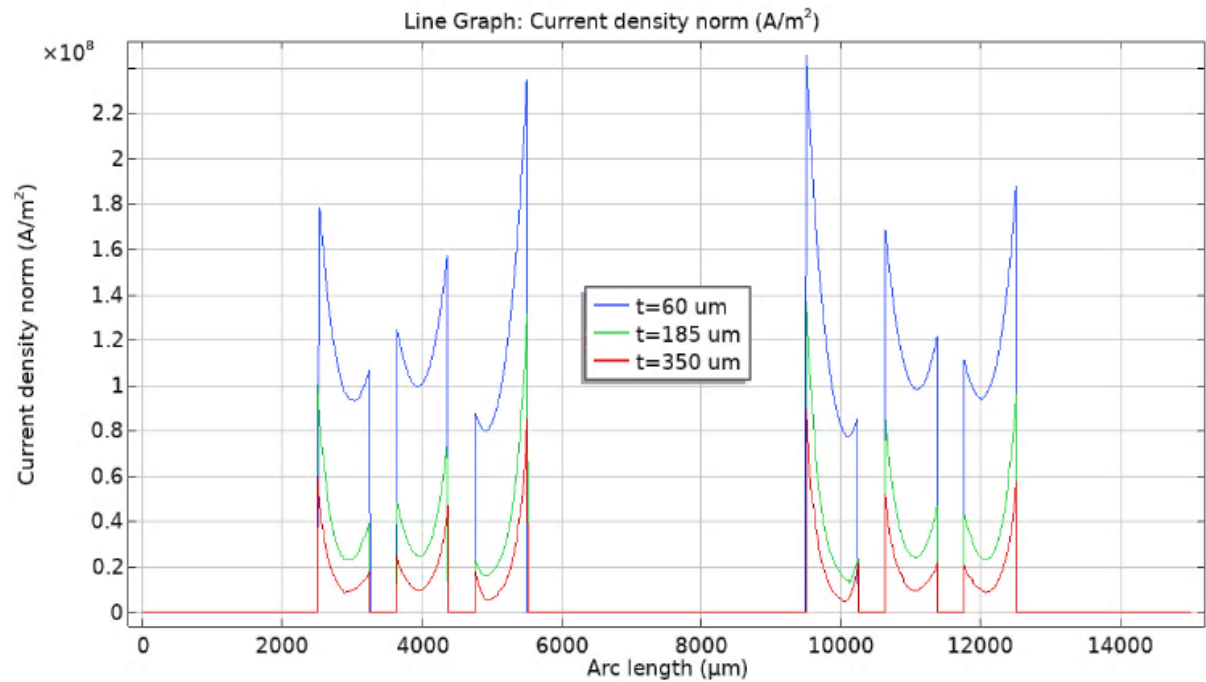
knowing the maximum value of the current flowing in the conductor, and the sections of the conductors studied, we calculated their current densities in order to compare the theoretical results ( $t=60\mu\text{m}$ ,  $24.82\times 10^7 \text{ A.m}^{-1}$ ); ( $t=185\mu\text{m}$ ,  $8.05\times 10^7 \text{ A.m}^{-1}$ ); ( $t=350\mu\text{m}$ ,  $4.25\times 10^7 \text{ A.m}^{-1}$ ) with the respective simulated densities.  $J_{\text{moy}}=17.728\text{A/m}^2$ ,  $5.75 \text{ A/m}^2$ ,  $3.035 \text{ A/m}^2$ . Results of simulations are presented in figures (II.13) and (II.14).

Figure (II.14) shows the distribution of the current density along the previously mentioned arc length. The same curve shape is observed in all cases with different values.

We also see higher current densities in the edges of the conductors facing the internal diameter of the spiral coil, this is due to the inverse proximity effect.

A direct proximity effect is manifested by higher current densities on the edges far from other adjacent conductors. Inside conductors, the current density is lower, except for the conductor of thickness  $t=60\mu\text{m}$  which shows a high density compared to the other two.

The current density is almost zero in the internal diameter and in the inter-turn spaces, which indicates that the parasitic currents resulting from the inter-turn capacitive effects are negligible.



**Figure II. 14:** Simulations of the current density norm according to the arc length mentioned in figure II.12 (c)

### 6.2.3. Simulation of AC losses for different conductor thicknesses

The copper losses in the magnetic coils depend on the geometric parameters of the inductor and the applied frequency. At high frequency, the proximity effect and the skin effect cause

uneven current distribution in the conductor, increasing its effective resistance. This makes their analytical modeling quite a difficult task.

For computing the losses of inductor under AC current and AC magnetic field, H-formulation is one of the most suitable methods for computing eddy-current losses [29]. The H-formulation consists of Maxwell Ampere's Law (II.20), Faraday's Law (II.21), Constitutive Law (II.22), Ohm's Law (II.23) and E-J power Law (II.24) [13]:

$$\nabla \times H = J \quad \text{Equation (II.9)}$$

$$\nabla \times E = \frac{\partial B}{\partial t} \quad \text{Equation (II.21)}$$

$$B = \mu_0 \mu_r H \quad \text{Equation (II.22)}$$

$$E = \rho J \quad \text{Equation (II.23)}$$

$$E = E_0 \left( \frac{J}{J_c} \right)^n \quad \text{Equation (II.24)}$$

Where J is the current density, H is the magnetic field intensity, B is the magnetic flux density, E is the electric field,  $\mu_0$  is the permeability of free space,  $\mu_r$  is the relative permeability,  $\rho$  is the resistivity,  $E_0$  is the characteristic electric field,  $J_c$  is the critical current density and n is the power factor.

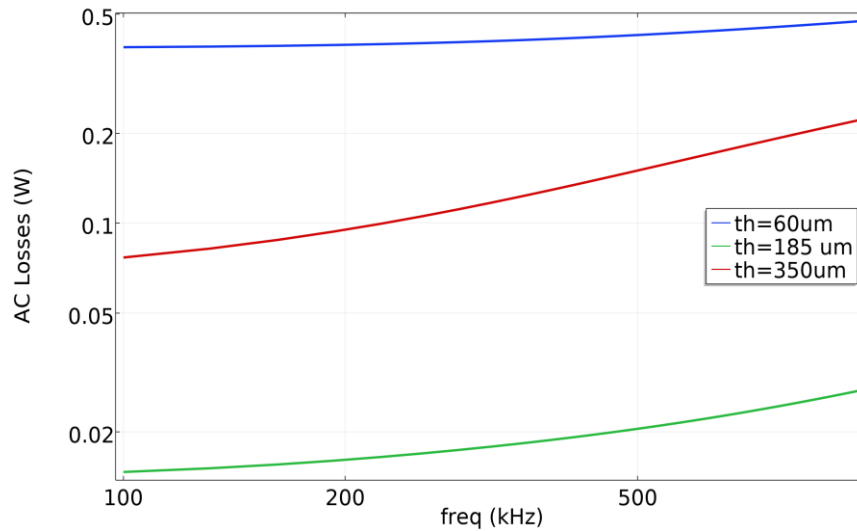
The general form of partial differential equation which includes the equations (II.20 to II.24) is II.25. Equation (II.25) is the E-J general power law.

$$\frac{\partial(\mu_0 \mu_r H)}{\partial t} + \nabla \times (\rho \nabla \times H) = 0 \quad \text{Equation (II.25)}$$

This partial differential equation was solved by COMSOL Multiphysics.

The simulation results for three different thicknesses samples are presented in Figures (II.15) and (II.16).

Figure (II.15) illustrate the AC losses in watt of the inductor according to the frequency. We notice that the eddy-current AC losses of copper for the thicknesses  $t=60\mu\text{m}$  and  $t=360\mu\text{m}$  are much higher. For the thickness  $t=185\mu\text{m}$  equal to  $2\sigma$ , the AC losses are very small.

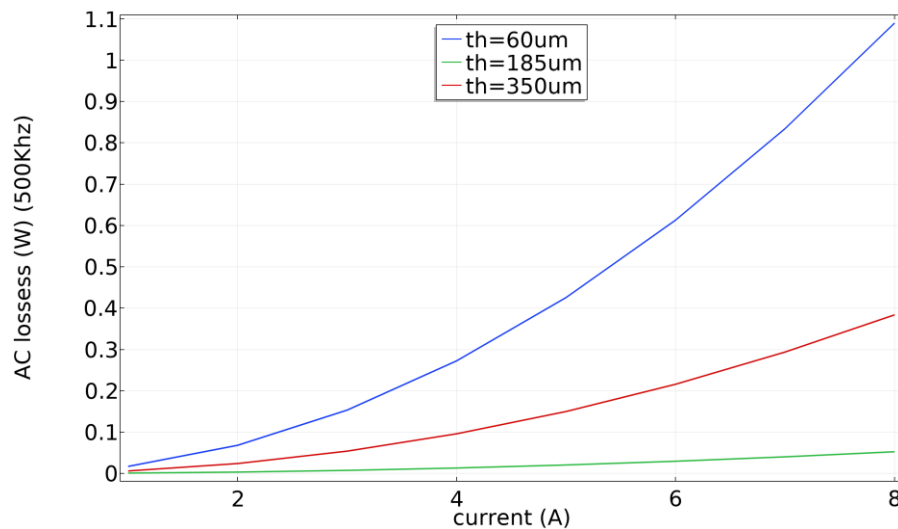


**Figure II. 15:** The AC losses of the single layer coil for different conductor thickness

Figure (II.16) shows the variation of the power losses according to the current flowing in the inductor for the three suggested thicknesses. These curves are simulated at the operating frequency  $f = 500\text{KHz}$ . Significant power loss is recorded for  $t = 60\mu\text{m}$  and  $360\mu\text{m}$ , while the inductor geometry with a thickness of  $185\mu\text{m}$  is relatively better because it shows exemplary power conservation.

We also note that for the thicknesses  $t = 360\mu\text{m}$  and  $t = 60\mu\text{m}$ , the power losses increase rapidly when the current increases, while for the thickness  $t = 185\mu\text{m}$  ( $t = 2\phi$ ), the power losses are very insensitive to the variation of current.

Through these results, we conclude that the AC power losses are optimal when thickness is equal to  $2\phi$ .



**Figure II. 16:** AC losses in planar inductor according to the inductor flowing current

#### 6.2.4. The inductance

The inductance is generally expressed by the ratio of the magnetic flux on the current intensity passing through the coil. To plot the inductance curve of the single layer inductor, for different values of the conductor thickness, we use the COMSOL software. The simulation is based on the expression II.26, where  $W_m$  is the total magnetic energy in the simulated air box by COMSOL multiphysics.

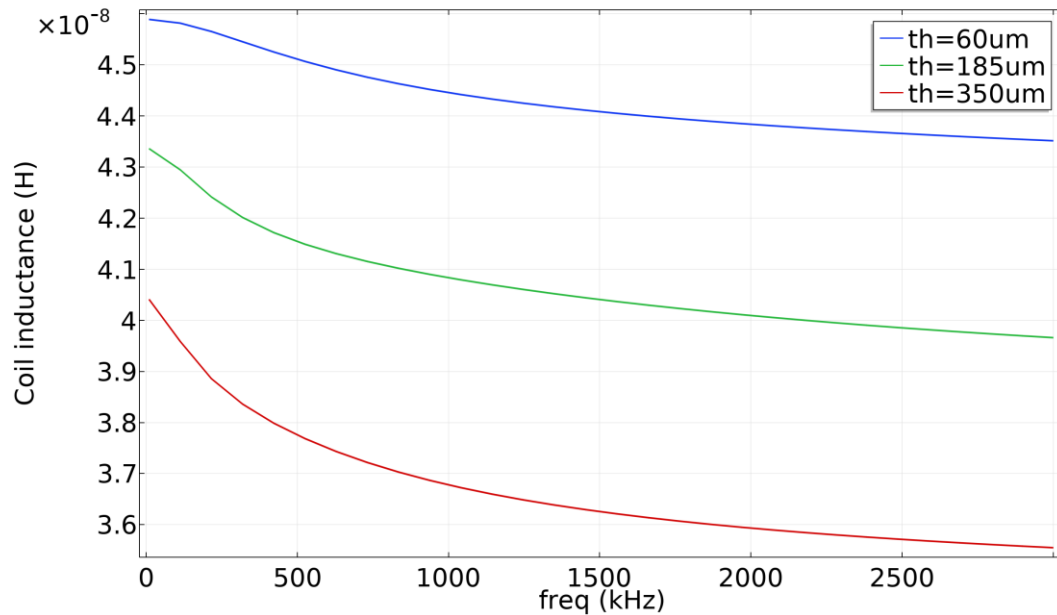
$$L = 2W_m / I^2 \quad \text{Equation (II.26)}$$

Figure II.17 illustrates the behavior of inductance according to the frequency for different conductor thicknesses. We find that the largest value of inductance is associated with the smallest thickness.

Table II.9 presents the measured inductance values for different thicknesses in DC and at 500 Khz.

Thickness	60μm	185μm	360μm
DC	$8.58 \times 10^{-8}$ H	$8.33 \times 10^{-8}$ H	$8.04 \times 10^{-8}$ H
500 Khz	$8.51 \times 10^{-8}$ H	$8.11 \times 10^{-8}$ H	$7.77 \times 10^{-8}$ H

**Table II.9:** The measured inductance values according to the thickness and applied frequency.



**Figure II. 17:** The inductance curves of single layer inductor for different thicknesses

### 6.2.5. The inductor AC resistance

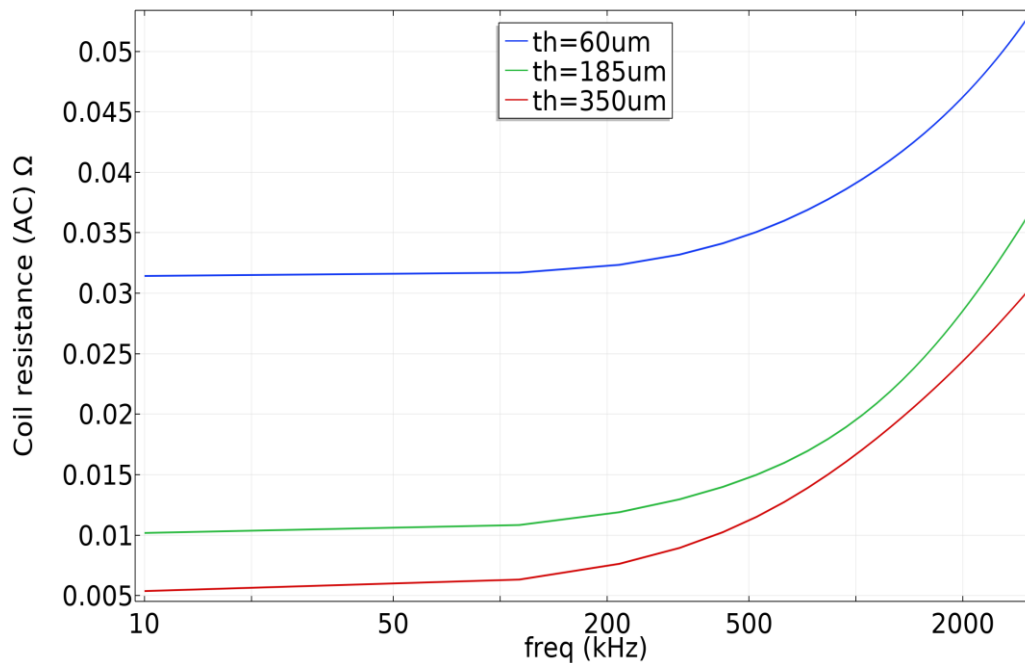
The numerical magnetostatic simulation calculates both the inductance and the resistance. Dealing with high frequency, the skin effects and capacitive effects become substantial. The skin effect modifies the current distribution in the conductor, so the resistance increases and the inductance also changes.

The equivalent AC resistance ( $R_{AC}$ ), which takes into account skin and proximity effects at the switching frequency, is required to calculate the joule losses for the high-frequency ripple. There is no analytical formula for calculating  $R_{AC}$  since the magnetic field in the inductor affects the distribution of current in the conductor [30].

Table II.10 demonstrates the measured values of the Ac resistance for suggested thicknesses according to the applied frequency.

Thickness	60 $\mu$ m	185 $\mu$ m	360 $\mu$ m
DC	0.03142 $\Omega$	0.01010 $\Omega$	0.005363 $\Omega$
500 Khz	0.03480 $\Omega$	0.01474 $\Omega$	0.01119 $\Omega$

**Table II. 10:** The inductor resistor values according to the thickness and applied frequency.



**Figure II. 18:** The AC resistance of the single layer planar inductor

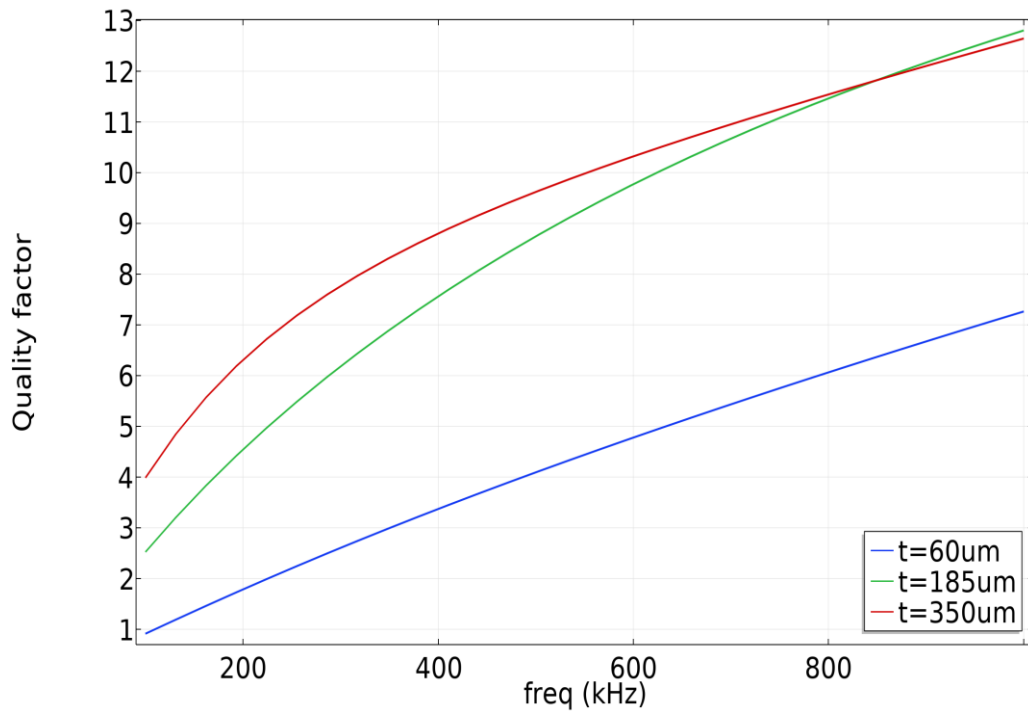
Figure 18 shows that the resistance (AC) increases with the frequency, because the increase of frequency leads to the reduction of the skin thickness and the increase of the conductor resistance, which favours losses by joule effects.

We also note that the resistance (AC) increases when the conductor thickness decreases, because reduction of the thickness reduces its section, which leads to more important current density and an increase of the conductor resistance.

### 6.2.6. The quality factors

The analysis of figure II.19 reveals that the lowest quality factor is recorded for the thickness of 60  $\mu\text{m}$ , which might be explained by the high Ac resistance caused by the small conductor section area, as well as the non-uniform current distribution caused by the applied frequency and proximity effect (see figure 13 d).

The values of the quality factor measured at the frequency 500 KHz for the respectively thicknesses [60 $\mu\text{m}$ -185 $\mu\text{m}$ -360 $\mu\text{m}$ ] are [4.09 - 8.74 - 9.61]



**Figure II. 19:** Variation of the Quality factor of the single layer planar inductor

### 6.2.7. Results interpretation

In the literature, the condition  $t \leq \delta$  or  $w \leq \delta$  is used to circumvent the skin effect and minimize the losses by Joule's effect. When we adjust the width  $w$ , three geometric parameters

change: the internal diameter  $D_{in}$  or external diameter  $D_{out}$ , and the distance between turns  $s$ . So, it is preferable to take the condition  $t \leq \delta$

The condition  $t \leq \delta$  is equivalent to  $(t < \delta \text{ or } t = \delta)$ , is it preferable to choose  $t < \delta$  or else  $t = \delta$ ? The study presented in this chapter II, allowed us to select the optimal condition.

By using the software COMSOL multiphysics, we studied the behaviour of parameters which affect the reliability and the quality of the planar inductor operating. These parameters are: AC resistance, inductance and the quality factor. The simulations were done for different conductor thicknesses “t”, [ $t=60\mu\text{m}$  ( $t < \delta$ ),  $t=185\mu\text{m}$  ( $t = \delta$ ) and  $t=360\mu\text{m}$  ( $t > \delta$ )].

In order to choose the optimal thickness between  $t < \delta$  and  $t = \delta$  we have grouped the obtained results in Table II.11.

Thickness	<b>60<math>\mu\text{m}</math></b>	<b>185<math>\mu\text{m}</math></b>
AC resistance	0.03480 $\Omega$	<b>0.01010 <math>\Omega</math></b>
L inductance	<b>8.51 x 10<sup>-8</sup> H</b>	<b>8.11 x 10<sup>-8</sup> H</b>
Quality factor	<b>4.09</b>	<b>8.74</b>

**Table II. 11:** The measured values according to different thicknesses at 500KHz

The results showed that the thickness  $t=60\mu\text{m}$  ( $t < \delta$ )  $\mu\text{m}$  gives the largest inductance value, but at the expense of a higher AC resistance and a very low-quality factor.

After this comparative analysis, we conclude that the thickness  $t < \delta$  presents the lowest quality factor, and a non-uniformity of the current density due to the significant proximity effects, so this thickness is rejected. So,  $(t = \delta)$  is the best condition to consider when designing the conductor's section of a planar inductor

## 7. CONCLUSION

In this chapter, we have made the sizing of an integrated planar inductor model for the DC-DC boost converter. According to the different numerical simulations, we have been able to observe the behaviour of the several important inductor's parameters (series resistance, quality factor, power losses, current density, inductance, leakage current). These parameters have to be well taken into account in order to implement an optimum design for planar magnetics.



The simulations also showed that the conductor thickness has a significant impact on the performance of the inductor, and allowed us to choose the optimal condition between  $t \prec \delta$  and  $t = \delta$ . In conclusion, a very thin winding is to avoid.

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# Chapter III

## Choice of the Optimal Gap of the Dual-layer Inductor

## 1. INTRODUCTION

Using the data from specifications, we have calculated in chapter II the inductance value necessary for the operation of the Boost converter. However, the calculated value was greater than the measured one by the COMSOL multiphysics software.

To resolve this problem, we added a second coil similar to the first. This second coil was placed above the first in order to take advantage of the mutual inductance and increase the inductance value. We named this structure “The dual-layer inductor”.

To minimize energy losses and ensure the proper functioning of the dual-layer inductor, the space (gap) between the two stacked coils must be studied with precision. In order to choose the optimal gap, we devoted this third chapter to the study of the gap and its influence on the operating parameters of the dual-layer inductor, such as: series resistance, energy losses, inductance and the quality factor.

The influence of the gap on the electromagnetic parameters has also been studied. The parameters studied are: current density, magnetic field and flux, leakage currents and displacement electric field.

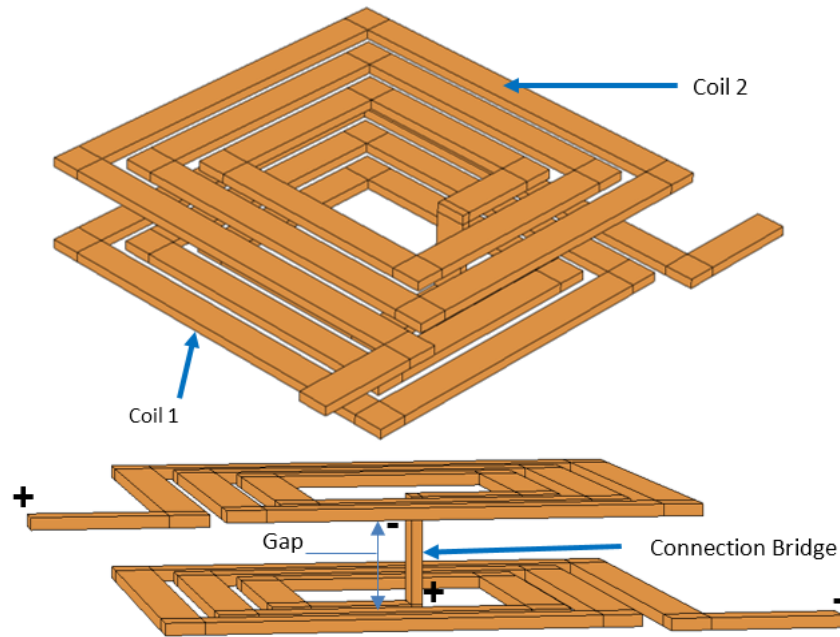
To accomplish this study, we used the simulation software COMSOL Multiphysics. The results obtained were commented, and the choice of the optimal gap was justified.

## 2. DUAL-LAYER SQUARE PLANAR SPIRAL INDUCTOR

To improve the inductance value and increase the magnetic energy, we placed a second planar coil in series above the first, as shown in figure III-1. On the last turn, a connecting bridge connects both planar coils. The coils were intentionally placed in this position to take advantage of the positive value of mutual inductance. The overall inductance is given by equation (III.1). Where  $L_T$  is the total inductance of the inductor presented in figure III.1,  $L_1$ ,  $L_2$  represents the self-inductance for (coil 1) and (coil 2), respectively.  $M$  is the mutual inductance generated by each coil.

The direction of current flowing in the coils determines the sign of mutual inductance. If the electrical current is flowing in the same direction for both coils, it will take a positive sign, and if it is flowing in opposite directions, it will take a negative sign [1-3].

$$L_T = L_1 + L_2 \pm 2M \quad \text{Equation (10)}$$



**Figure III. 1:** 3D presentation of the dual- layer inductor geometry without magnetic core  
(two different views angles)

The mutual inductance value for serial inductors depends mainly on their position and the distance between them (gap). It is known that this mutual inductance takes higher values for low gap due to the interaction of the magnetic flux generated between the two coils, which produces a relatively large electromagnetic field.

### 2.1. Impact of the gap on the inductance value

In the attempt to comprehend the deviations of this electromagnetic field, depending on the distance between these two square planar coils in series, we have numerically simulated the electromagnetic field of the geometry shown on figure III-2 for different gaps taken in interval  $I = [60 \mu\text{m}; 1500 \mu\text{m}]$ .

The results of simulation presented by figure III.2, show the evolution of the inductance  $L_T$  of the suggested geometry in the interval  $I$ .

Simulated results clearly show that when the gap between the two coils increases, the overall inductance decreases. After the curve analysis, it was concluded that the variation is not linear.

The highest overall inductance  $L_T$  value is recorded at the smallest gap, when the magnetic interaction is at its maxima. However, the minimum  $L_T$  value is reached at some gap where the mutual inductance is cancelled altogether; in this case, we can say that the two coils are

magnetically separated, and the equivalent inductance is equal to the sum of coils self-inductances.

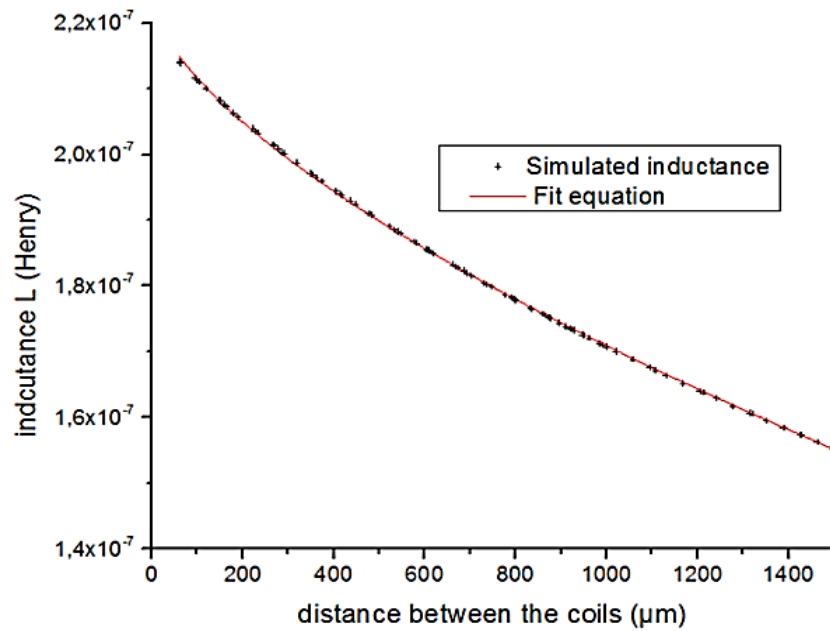
Following the analysis of the results, equation III.2 is formulated to characterise the behaviour of the  $L_T$  overall inductance according to the gap. Where  $D_g$  is the gap distance separating the coils, a, b and c are the coefficients presented in table III.1. Expression III.2 is graphically represented by the red curve in figure III.2. It fits 98% of the simulated results.

The coefficients a,b,c could be different for the same inductor geometry with different geometrical parameters.

$$L_T = a + b \times (D_g)^c \quad \text{Equation (III.2)}$$

a	b	c
2,23508E-7	-6,105E-10	0,64518

**Table III. 1:** Reached expression coefficients.

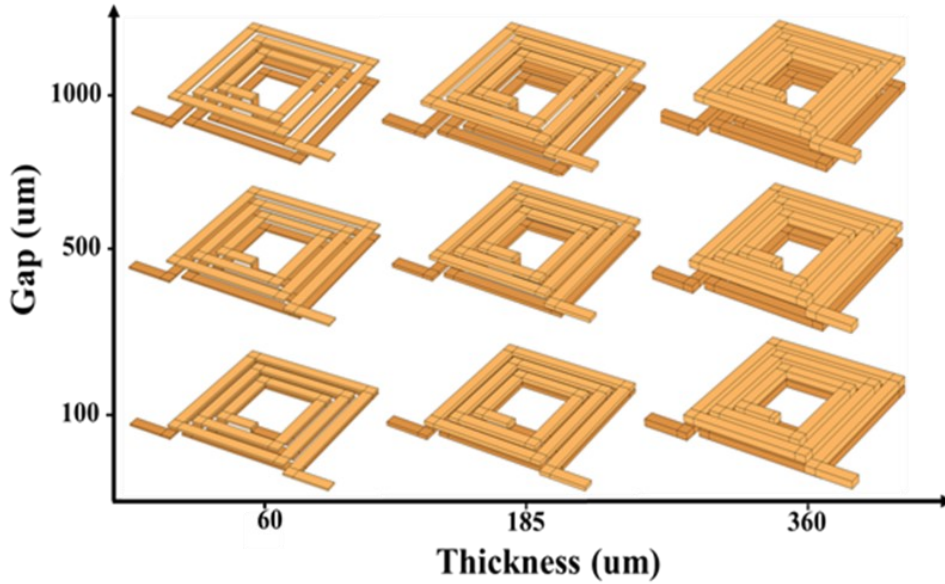


**Figure III. 2:** The impact of the gap on the overall inductance.

### 3. THE EFFECT OF THE CONDUCTOR THICKNESS AND THE GAP ON THE DUAL-LAYER INDUCTOR.

We have seen that the t conductor thickness and the  $D_g$  gap strongly influence the inductance value and its behaviour, therefore we propose to study the impact of the combination between these two parameters on the inductor performances.

For the sake to opt of the proper inductor with optimal properties and low losses, we performed a numerical study for nine different inductors with the following parameters: Thickness: [90-185-360] /gap: [100, 500, 1000]. The proposed geometries are presented in figure III.3.

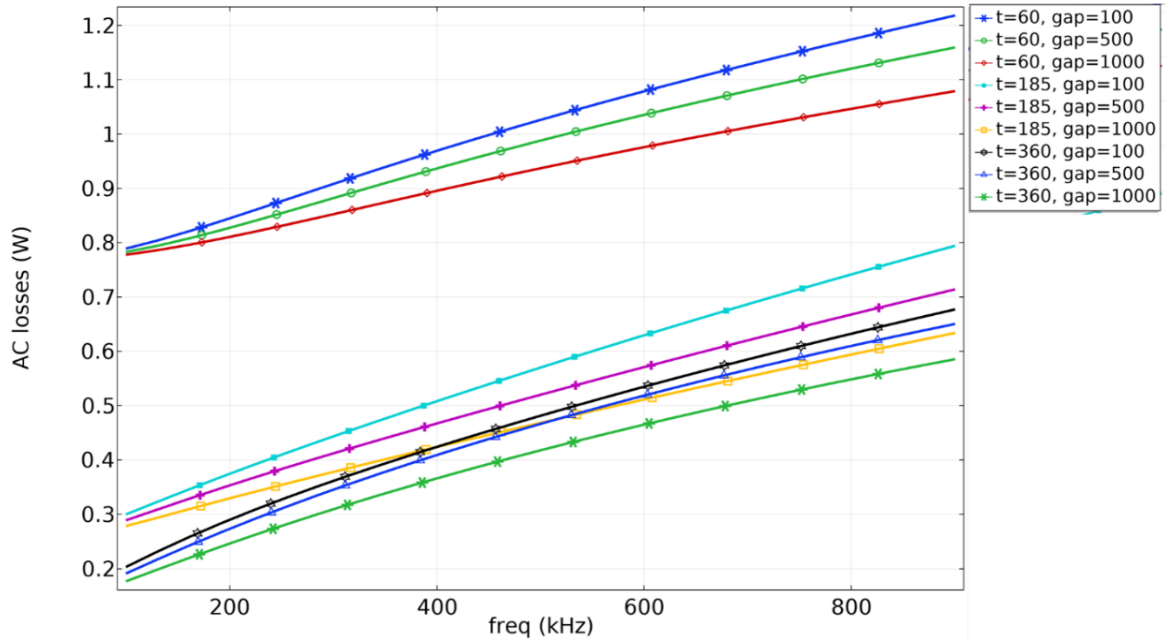


**Figure III. 3:** The dual layer inductor with different conductor thicknesses and gaps

### 3.1. Dual layer inductor AC losses

Figures III.4 and III.5 demonstrate the numerical simulation results of AC losses for the nine indicated cases, using the finite element approach. Through the results, we can observe in figure III.4 that the inductor with a 60  $\mu\text{m}$  conductor thickness has high power losses compared to the other cases. This could be explained by the inductor's AC resistance owing to the small conductor section, which causes more current flows via the parasite coupling capacitance between the two coils. Due to these results, it is unlikely to select inductor with a thin thickness. These results agree with those of the single layer inductor.

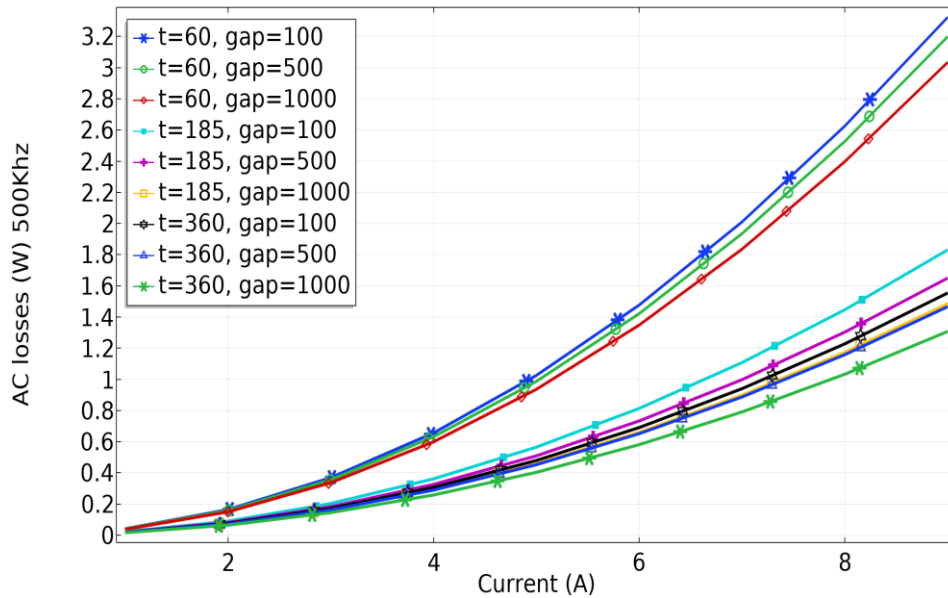
We notice that even the gap affects the AC energy losses, but it doesn't have as much influence as the conductor thickness.



**Figure III. 4:** AC losses for dual layer inductor with different gaps and thicknesses

Figure III.5 shows the variation of power losses according to the inductor's flowing current at the operating frequency (500 kHz).

A Significant Power loss is recorded for inductors with  $t = 60\mu\text{m}$  compared to other cases. This is due to the leakage currents that increase with the current density, in particular for the small conductor section.



**Figure III. 5:** The AC losses in dual layer inductor according to the current for different thicknesses and gaps



### 3.2. The inductance of the dual-layer inductor

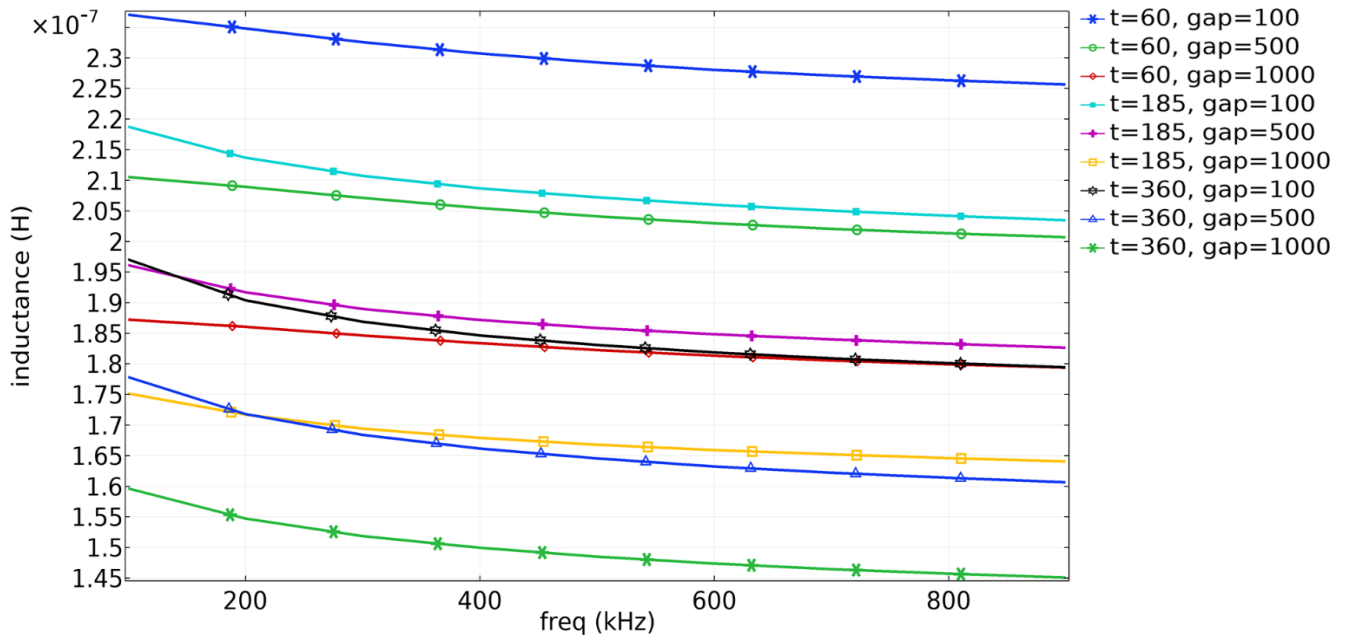
The variation of the inductance according to the frequency for the nine selected cases is depicted in Figure III.6. This numerical simulation results show that, the inductance value differs for each case.

Figure III.6 shows in particular the influence of the gap on the inductance value. We find that the highest inductance values are attributed to the smallest gap. This is due to the mutual inductance which becomes more important when the gap decreases. These results confirm those of figure III.2.

For more precision, we have measured the different inductance values for suggested thicknesses and gaps at DC (Direct Current) and 500 KHz (Table III.2).

Gap Dg \ Thickness t	100μm		500μm		1000μm	
	DC	500KZ	DC	500Khz	DC	500Khz
60μm	$2.23 \times 10^{-7}$ H	$2.29 \times 10^{-7}$ H	$2.11 \times 10^{-7}$ H	$2.04 \times 10^{-7}$ H	$1.87 \times 10^{-7}$ H	$1.82 \times 10^{-7}$ H
185μm	$2.23 \times 10^{-7}$ H	$2.07 \times 10^{-7}$ H	$1.99 \times 10^{-7}$ H	$1.85 \times 10^{-7}$ H	$1.77 \times 10^{-7}$ H	$1.66 \times 10^{-7}$ H
360μm	$2.06 \times 10^{-7}$ H	$1.83 \times 10^{-7}$ H	$1.85 \times 10^{-7}$ H	$1.64 \times 10^{-7}$ H	$1.65 \times 10^{-7}$ H	$1.48 \times 10^{-7}$ H

**Table III. 2:** The measured inductance values for different thicknesses and gap



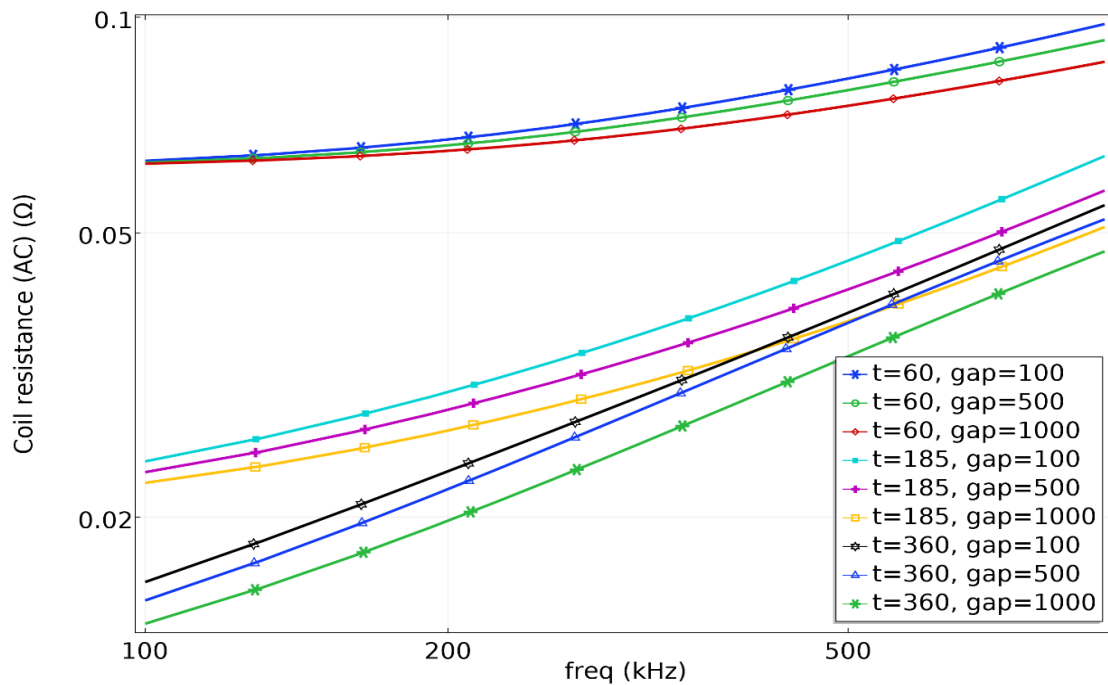
**Figure III. 6:** The inductance of a dual layer inductor for different thicknesses and gaps

### 3.3. The dual-layer inductor resistance

Figure III.7 presents the variations of the series resistance of the dual-layer inductor for different gaps and thicknesses, also, its variation according to frequency. A significant resistance is recorded for the thickness  $t = 60\mu\text{m}$ . This is explained by the fact that, in the case of a very thin thickness, the series resistance of the dual-layer inductor is the association of three resistances: the high Ac resistance caused by the small conductor section, the resistance against leakage currents through the coupling capacitance between the two coils, and also the resistance due to the uneven current distribution caused by the proximity effect. The series resistance at DC and 500 KHz are presented in table III.3. The increase in frequency leads to an increase in the resistance of dual layer inductor (Figure III.7).

Gap Dg \ Thickness t	100 $\mu\text{m}$		500 $\mu\text{m}$		1000 $\mu\text{m}$	
	DC	500KZ	DC	500Khz	DC	500Khz
60 $\mu\text{m}$	0.0610 $\Omega$	0.082 $\Omega$	0.0612 $\Omega$	0.079 $\Omega$	0.0614 $\Omega$	0.075 $\Omega$
185 $\mu\text{m}$	0.0197 $\Omega$	0.045 $\Omega$	0.0198 $\Omega$	0.041 $\Omega$	0.0198 $\Omega$	0.037 $\Omega$
360 $\mu\text{m}$	0.0101 $\Omega$	0.038 $\Omega$	0.0101 $\Omega$	0.037 $\Omega$	0.0101 $\Omega$	0.033 $\Omega$

**Table III. 3:** The measured resistances values of the dual layer inductor, for different gaps and thicknesses.



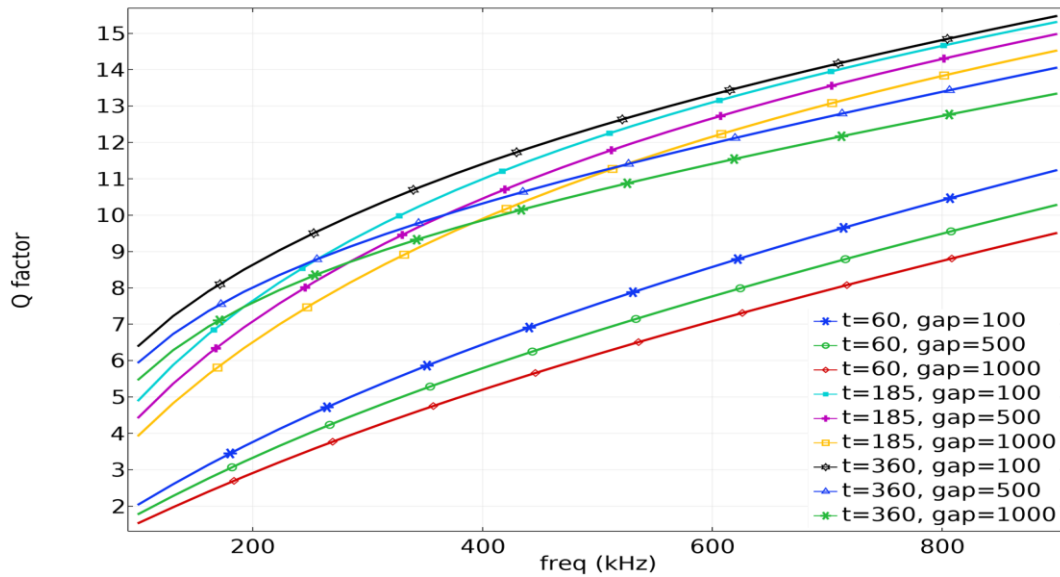
**Figure III. 7:** The dual-layer inductor resistance for different gaps and thicknesses.

### 3.4. The quality factors

The analysis of figure III.8 and table III.4 show that all gaps accompanied with a thickness of 60  $\mu\text{m}$  have the lowest quality factor, although the 60  $\mu\text{m}$  thickness shows the greatest inductance values (Table III.2, Figure III.6). This is due to the high coil AC resistance (Figure III.7).

Gap Dg \ Thickness t	100 $\mu\text{m}$	500 $\mu\text{m}$	1000 $\mu\text{m}$
60 $\mu\text{m}$	7.55	6.82	6.17
185 $\mu\text{m}$	12.14	11.65	11.12
360 $\mu\text{m}$	12.43	11.19	10.65

**Table III. 4:** The quality factor values of the dual layer inductor at 500 KHz



**Figure III. 8:** The quality factor of the dual-layer inductor for different gaps and thicknesses

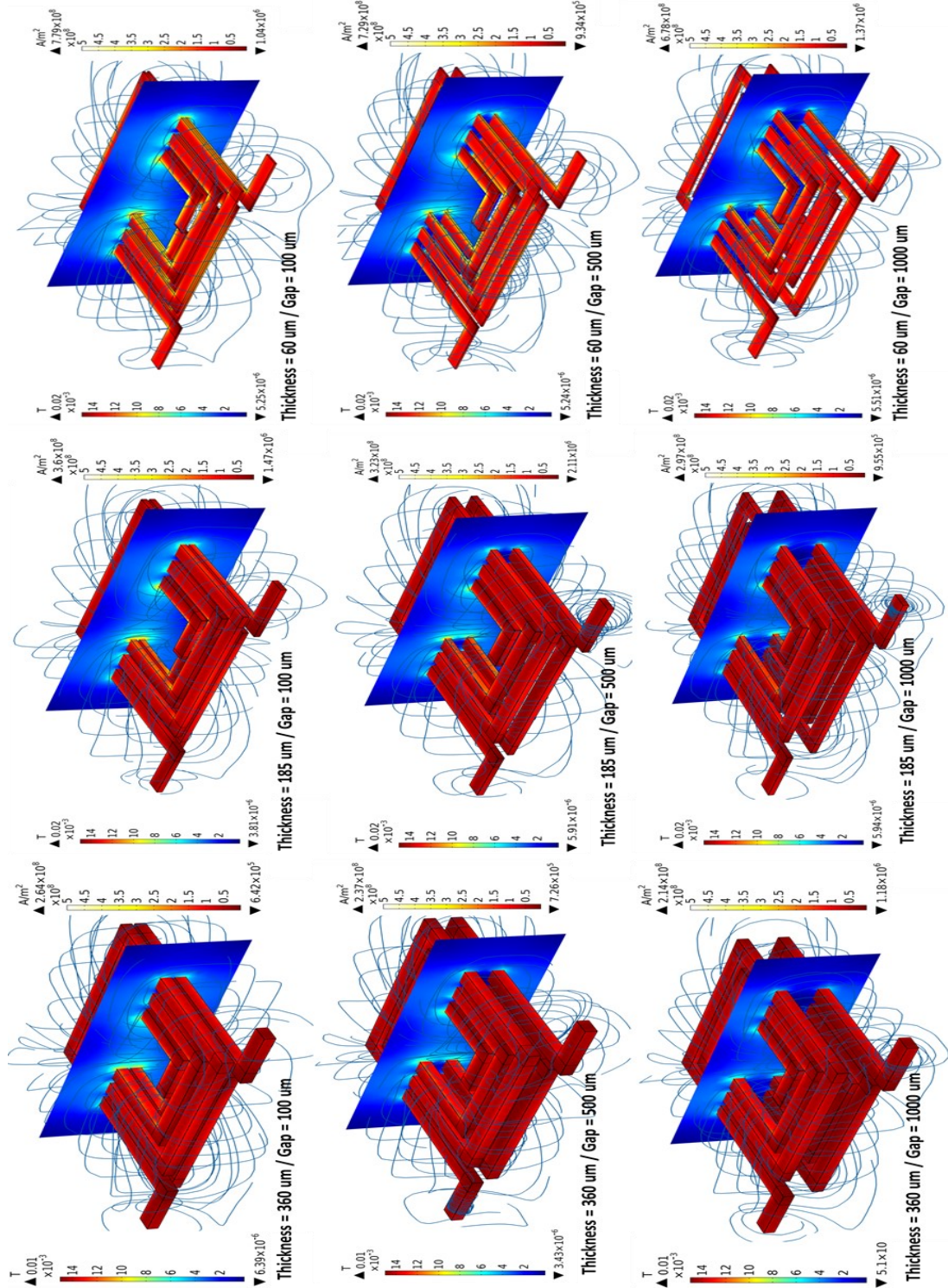
## 4. INDUCTOR ELECTROMAGNETIC INVESTIGATION

In this part, we present the simulation results of different electromagnetic effects such as the current density in the conductive winding, the distribution of the magnetic field lines and the magnetic flux distribution.

### 4.1. Magnetic flux and magnetic field lines

Figure III.9 depicts the distribution of magnetic flux density and the magnetic field lines in the dual-layer inductor with varying parameters (thickness and gap). The nine figures show a good

distribution of magnetic field lines. We observe that the centre area of the dual-layer inductor registers the maximum value of the magnetic flux for all cases. It is due to the high concentration of magnetic field lines in this area. We therefore, conclude that the dual-layer planar model works correctly.



**Figure III. 9:** 3D view of the numerical simulation showing the current density and the magnetic flux distribution

## 4.2. Electrical density distribution in the dual-layer inductor

Figure III.9 in 3D visualization shows also, the current density distribution in the dual-layer inductor for different thicknesses and gaps.

For the smaller thickness of the conductor ( $60\text{ }\mu\text{m}$ ), we observe a higher current density in the edges of the conductors facing the internal diameter, its results from the inverse proximity effect and the higher magnetic flux density at the centre of the inductor. This phenomenon become less important for  $t=185\text{ }\mu\text{m}$ , then disappear for  $t=360\text{ }\mu\text{m}$ . Figures III-11 and III.13 give us more precision.

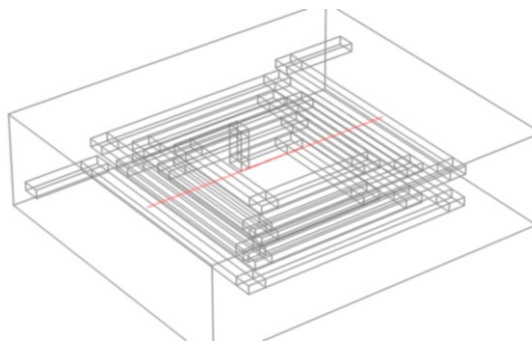
For the smallest gap ( $100\text{ }\mu\text{m}$ ) accompanied by the smallest conductor thickness ( $60\text{ }\mu\text{m}$ ), we observe a more accentuated direct proximity effect between the two stacked coils. This is due to the parasitic coupling capacitance between the two coils which becomes greater when they are closer. These phenomena become less important as the gap widens and the thickness  $t$  increases. These results confirm those of Figure III.4.

### 4.2.1. Horizontal view

To study the current density distribution inside the dual-layer inductor turns (Figure III.11), we went through the transverse section of the top coil (Figure III.10).

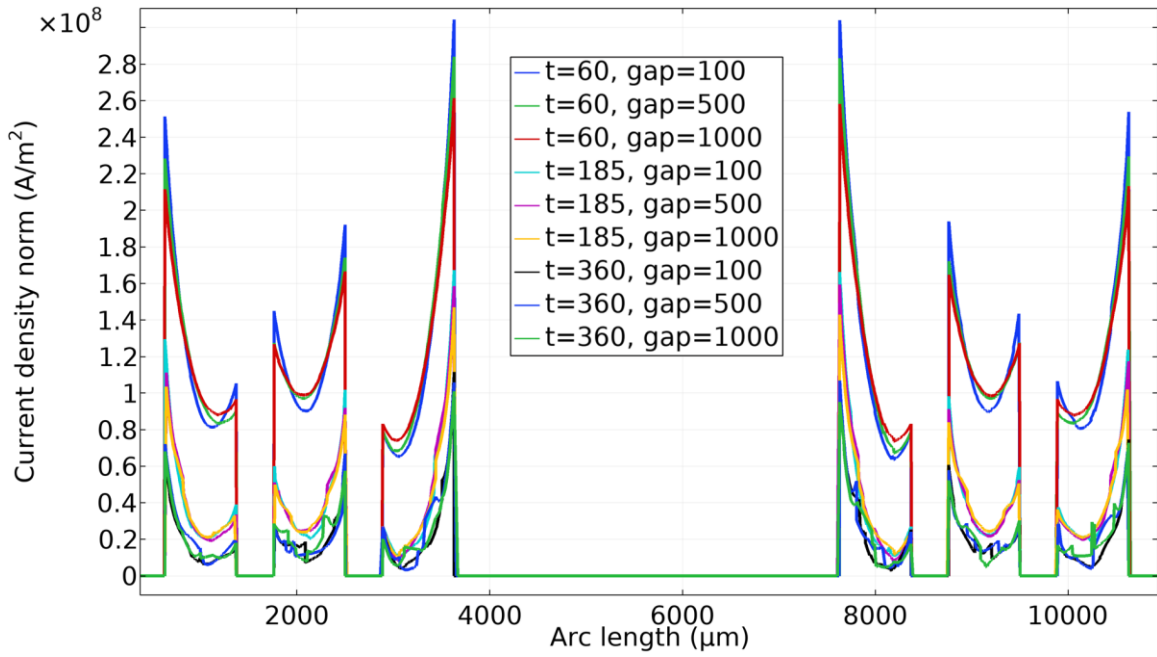
Figure III.11 confirms the absence of the skin effect for  $60\text{ }\mu\text{m}$  and  $185\text{ }\mu\text{m}$  thicknesses. A low current density is observed at the centre of the conductor for  $t = 360$ , it's due to the accentuated skin effect.

The direct proximity effect is present in the two outer spirals and the opposite effect in the inner, for all cases. These effects are very accentuated for the  $60\text{ }\mu\text{m}$  thickness presenting current peaks, which can lead to the heating of the conductor. The current density is zero between the turns and in the internal diameter area.



**Figure III. 10:** The horizontal arc passing through the upper coil



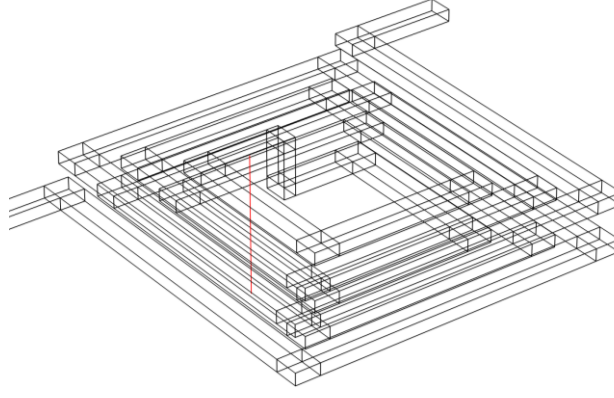


**Figure III. 11:** The electrical current distribution on top coil according arc presented in figure III.12

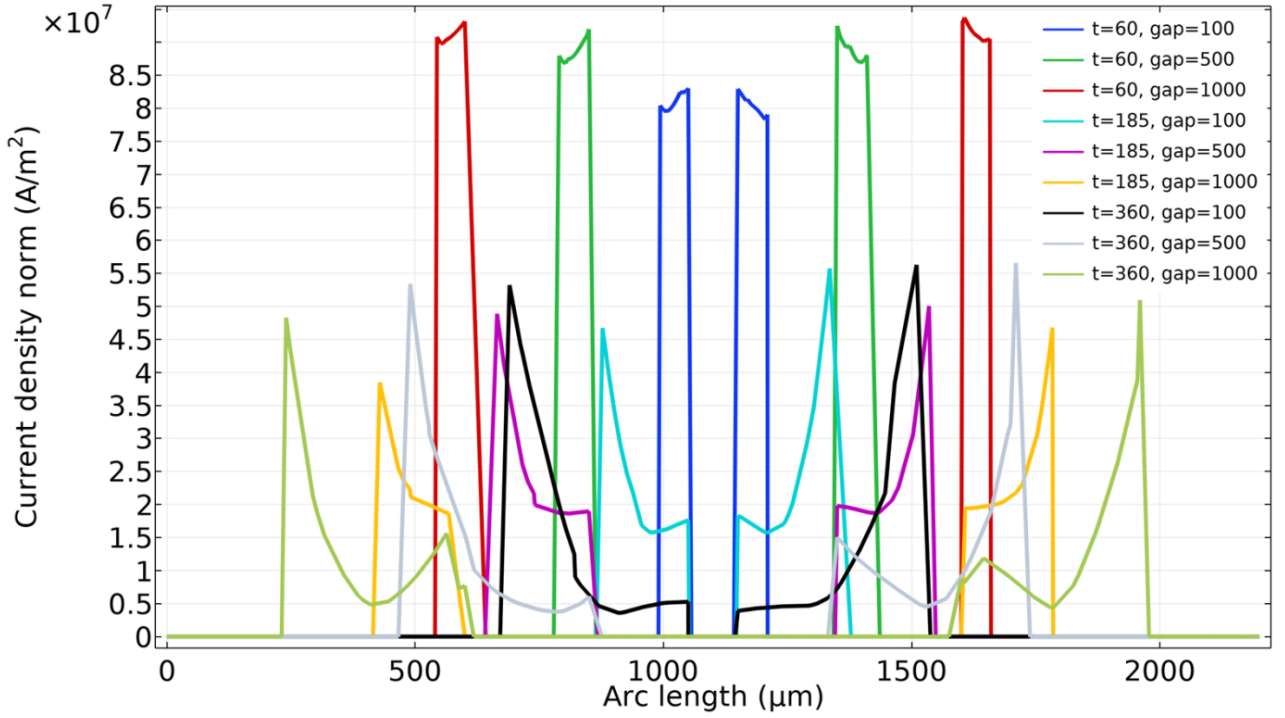
#### 4.2.2. Vertical view

To see the influence of the gap on the distribution of the current density inside the conductor, we realized figure III.13. This figure is realized according to the vertical section (Figure III.12) that passes through the segments of the external turns of both coils separated by the gap.

Figure III.13 shows a significant current density at the outer boundaries of the top and bottom coils for 185μm and 360μm conductor thicknesses. which is explained by the direct proximity effect. For the smallest thickness (60m), the current density is much greater because of the small conductor section. On the other hand, we notice a totally different behaviour for this thickness: the effect of direct proximity has disappeared to be replaced by a weak effect of inverse proximity although the current crossing the two coils circulates in the same direction. This behaviour is due to the parasitic coupling capacitance between the two coils that is large enough to cancel out the direct proximity effect.



**Figure III. 12:** The vertical arc that passes through the last turn of

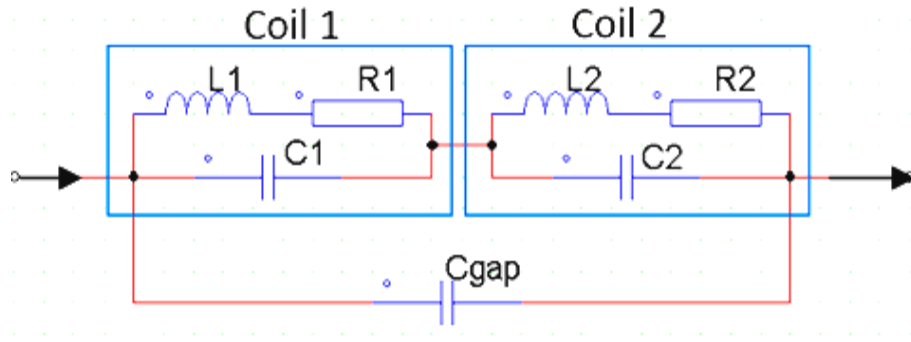


**Figure III. 13:** The electrical current distribution according to the arc length of figure III.12.

Before opting for the choice of the optimal gap and the optimal thickness, we first study the influence of the parasitic coupling capacitance between the two coils on the operation and efficiency of the dual-layer inductor.

#### 4.2.3. The parasitic capacitive effect

When selecting the gap, the parasitic coupling capacitance  $C_{gap}$  between the two coils must be taken into consideration, because this capacitance strongly affects the operation and efficiency of the inductor.  $C_{gap}$  is presented in the equivalent electrical circuit of Figure III.14.



**Figure III. 14:** Equivalent schematic of the dual layer inductor

$L1$  and  $L2$  are the self-inductances for each coil,  $R1$  and  $R2$  are the self-resistance of their conductors.  $C1$  and  $C2$  represent the inter-spire coupling capacities of each coil. They are given by equation III.3.

$$C1 = C2 = \varepsilon_0 \frac{l_t \cdot t}{s} \quad \text{Equation (III.3)}$$

The total length  $l_t$  of the conductor in a square spiral inductor is determined from formula III.4. By using data of Table II.7, we find  $l_t = 81.82 \text{ mm}$ . For the dual layer inductor,  $l_{td} = 2l_t + D_g$ ,  $D_g$  is the gap width.

$$l_t = 4n [d_{out} - (n - 1)s - nw] - s \quad \text{Equation (III.4)}$$

#### 4.2.3.1. Calculation of parasitic capacities

The value of this  $C_{gap}$  coupling capacitance is proportional to the region of interaction between the two coils as it's presented in figure III.15 and symbolised by  $A_i$ . Also,  $C_{gap}$ , strongly depends on the relative permittivity of the dielectric material. So, the choice of material is very important.

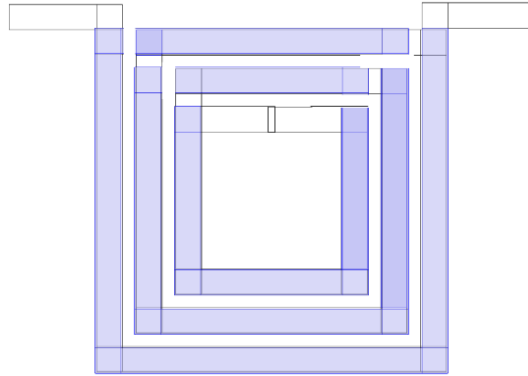
After long research in the literature on the best dielectrics used for planar inductors, we found that the Kapton-Polyimide is recommended, because it's extremely durable and provides a low dielectric loss over a wide frequency range and high breakdown voltage. Furthermore, an excellent balance of properties over a wide range of temperatures [4-5]. Its relative permittivity is about 3.85.



With a total length of the conductor  $l_t = 81.82 \text{ mm}$  and a width  $W = 470 \mu\text{m}$ , the calculated interaction area between the top and bottom coils is  $5.92 \times 10^7 \mu\text{m}^2$ . This area is constant in all cases. The value of  $C_{\text{gap}}$  can be calculated from equation III.5.

$$C_{\text{gap}} = \epsilon_0 \epsilon_r \frac{A_i}{D_g} \quad \text{Equation (11)}$$

We recall that  $D_g$  is the width of the gap separating the two coils.

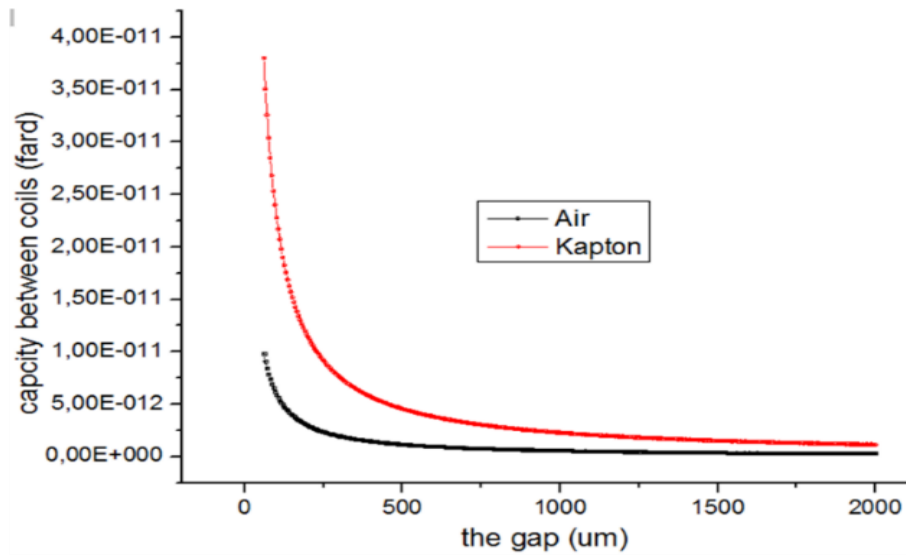


**Figure III. 15:** Top view of the interactive section between the two planar coils.

#### 4.2.3.2. Variation of coupling capacitance Gap according to the gap

To study the influence of the coupling capacitance  $C_{\text{gap}}$  on the efficiency of inductor, a comparison was done for two examples with and without Kapton by varying the gap.

Figure III.16 shows the collected findings as a curve. This curve can be interpreted according to two intervals. In the first,  $C_{\text{gap}}$  capacitance takes more important values for small gaps, in particular, with the insertion of the dielectric. This leads to an increase in the leakage electrical current between the two coils and a lower efficiency of the dual layer inductor. We notice, also that the  $C_{\text{gap}}$  capacitance varies sharply in response to the variation of the gap. Selecting a gap in this range is entirely ruled out.



**Figure III. 16:** Variation of Cgap capacitance according to the gap (with/without Kapton).

In the second interval, the Cgap capacitance takes smaller values, and the variation of the  $D_g$  gap has a less significant influence on the Cgap capacitance.

Although the value of the Cgap capacitance is slightly higher with the insertion of the Kapton, there is no technical way to avoid it because, it takes the role of support and isolation between the coils and avoids the dynamic instability of the dual-layer inductor.

The values of Cgap and the inter-turns capacitance  $C_s$  of each case are presented in Table III.5 and III.6. The values are calculated from previous formulas and confirmed by electrostatic numerical simulation.

Gap $D_g$	100 $\mu\text{m}$	500 $\mu\text{m}$	1000 $\mu\text{m}$
Cgap with kapton	2,02E-11 F	4,04E-12 F	2,02E-12 F
Cgap without	5,24E-12 F	1,05E-12 F	5,24E-13 F

**Table III. 5:** Cgap values for different gaps at 500KHz

Thickness $t$	60 $\mu\text{m}$	185 $\mu\text{m}$	360 $\mu\text{m}$
$C_s$	7,19E-14 F	2,21E-13 F	4,32E-13 F

**Table III. 6:**  $C_s$  values for different thicknesses at 500KHz

#### 4.2.3.3. Exploration of the leakage current by Cgap

The visualisation of the amount of leakage current through the parasite capacitance Cgap is required for the best gap selection. As a result, we used the PSIM software to simulate the

equivalent circuit of the dual-layer inductor shown in figure III.14 in order to observe each case's behaviour. The analysis was carried out by passing a 5 A average current through the dual-layer inductor's equivalent circuit. The 5A current is in accordance with the specifications (Table II.2).

We conducted a numerical simulation for the nine geometries of the examined situations applying Maxwell's equations III.6, III.7, III.8, and III.9 [6] to observe the electric displacement field DE and validate the obtained results.

$$\nabla \times H = J + \frac{\partial D_E}{\partial t} \quad \text{Equation (III.6)}$$

$$\nabla \times E = \frac{\partial B}{\partial t} \quad \text{Equation (III.7)}$$

$$\nabla \cdot D_E = \rho \quad \text{Equation (III.8)}$$

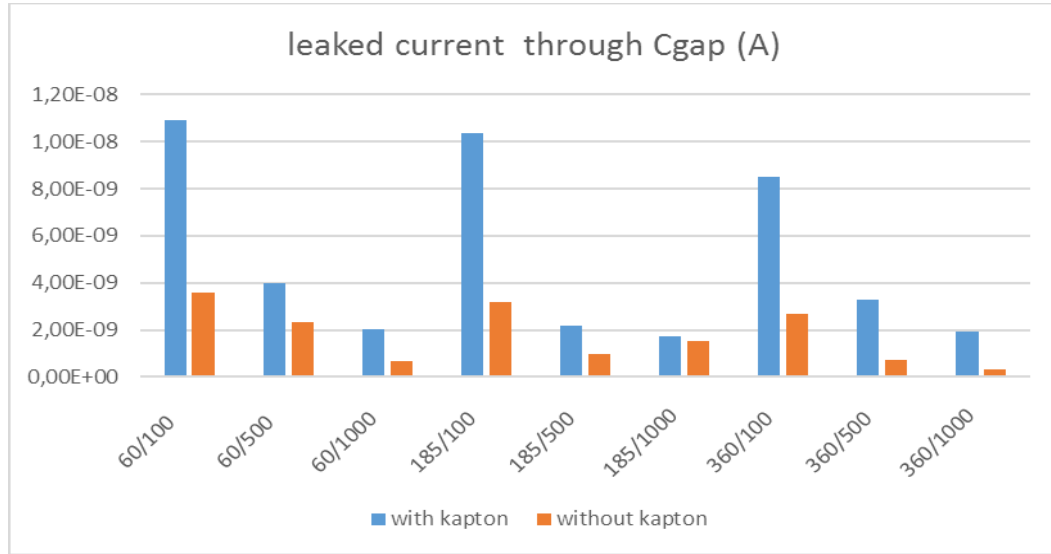
$$\nabla \cdot B = 0 \quad \text{Equation (III.9)}$$

Where E is Electric field intensity, D<sub>E</sub> is Electric displacement or electric flux density, H is Magnetic field intensity, B is Magnetic flux density, J Current density and ρ Electric charge density.

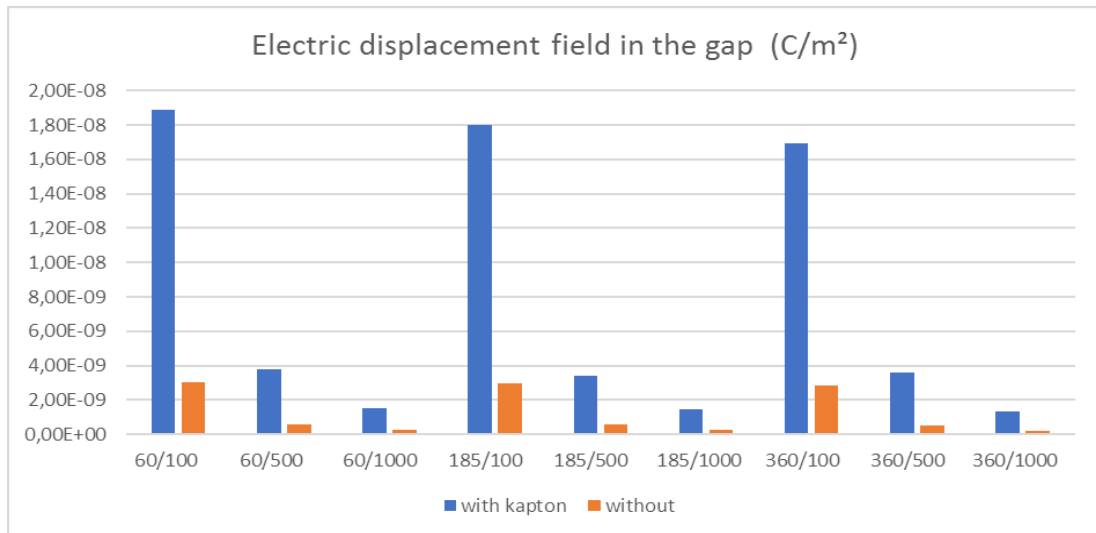
The simulation results of the electrical circuit of figure III.14 are represented in Figures III.17 and III.18.

The leaked current through Cgap capacitance (Figure III.17) takes the higher values for the smallest gap Dg=100μm (with and without Kapton). However, the gaps 500μm and 1000μm generate lower leakage currents.

The same results are observed in figure III.18 showing the electric displacement field in the capacitance Cgap. Both figures indicate that when the gap width is increased, leakage currents through Cgap are slowed down and become negligible when there is no Kapton.



**Figure III. 17:** Presentation of leakage current through  $C_{gap}$  for each case.



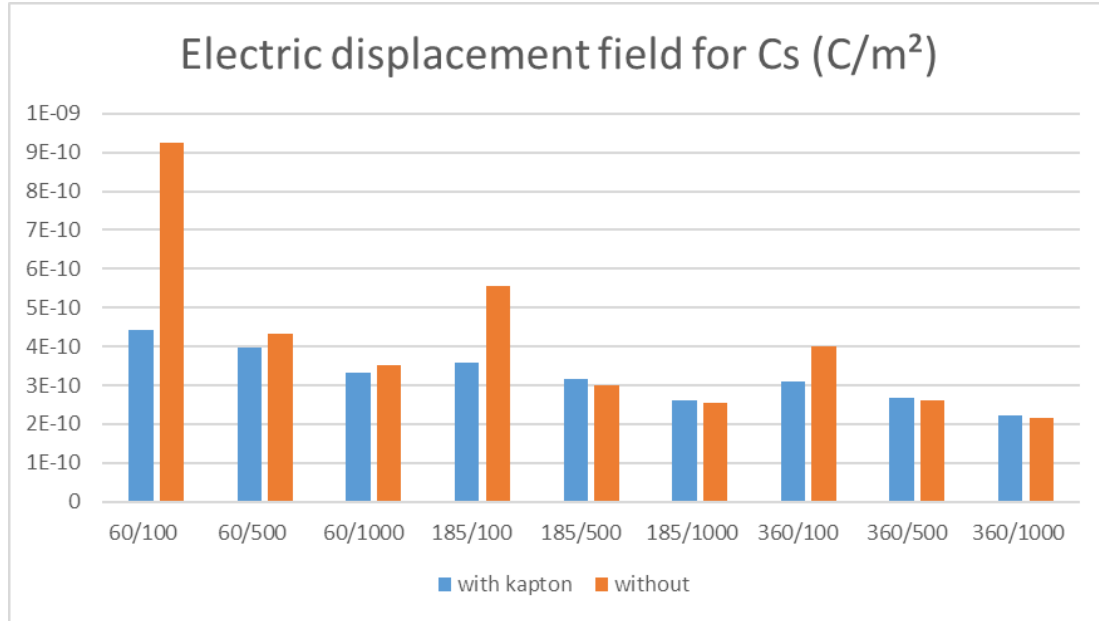
**Figure III. 18:** Presentation of electric displacement field in  $C_{gap}$ , result of numerical simulation of the dual-layer inductor

#### 4.2.3.4. Exploration the leakage current by $C_s$

We have done the same simulation to explore the leakage current through the inter-turns parasitic capacitance.

We observe in figure III.19 the electrical displacement field in the parasitic capacitance created between the inductor turns. This numerical simulation allows us to see the influence of the Kapton on the leakage current between the turns. The simulation is done for the top coil of the dual-layer inductor, with and without Kapton.

The obtained result show that a small width of the gap (100 $\mu\text{m}$ ) favors the electric field between the turns, in particular when there is no Kapton. Because when the dielectric of Kapton is placed between the two coils, the electric field in the gap becomes stronger (see figure III.18), on the other hand, the electric field between the turns weakens.



**Figure III. 19:** Presentation of electric displacement field in Cs, result of numerical simulation of the dual-layer inductor.

## 5. INTERPRETATION OF RESULTS AND CHOICE OF THE OPTIMAL DIMENSIONS OF THE THICKNESS AND THE GAP

### 5.1. Choice of the optimal thickness

A thickness of the conductor which satisfies the condition  $t = 60\mu\text{m} \prec 2\delta$ , certainly, it avoids the skin effect, but, generates several other parasitic effects which disturb the good functioning of the inductor. The harmful effects resulting from the thickness  $t \prec 2\delta$  are:

- A significant power loss compared to  $t = 180\mu\text{m} = 2\delta$  and  $t = 360\mu\text{m} \succ 2\delta$  (Figure III.4).
- The weakest quality factor is recorded for  $t \prec 2\delta$  (Figure III.8).
- $t \prec 2\delta$  presents a very accentuated proximity effect (Figure III.13).
- $t \prec 2\delta$  favours the circulation of leakage currents in the gap, in particular when there is a dielectric (Figure III.18).

Following these interpretations, the thickness  $t \prec 2\delta$  is rejected.

The thickness  $t \succ 2\delta$  favours the skin effect in the conductor (figure III.12). This phenomenon is to avoid, because it generates losses by Joules effect which heats the conductor and degrades the performances of the inductor. In addition to this defect, it presents the weakest value of inductance (Figure III.6). For these reasons,  $t \succ 2\delta$  is rejected.

The thickness  $t=2$  has a good quality factor (Figure III.8), better inductance compared to that of  $360\mu\text{m}$  (table III.2), low inter-turns parasitic capacitance (Table III.6), as well as a low leakage current through  $C_{\text{gap}}$  (figure III.18), in particular for  $500\mu\text{m}$  and  $1000\mu\text{m}$  gaps. For these reasons, we opt for a thickness  $t=180$ .

When dimensioning a spiral planar inductor, the conductor width and thickness must be well considered. It is known in literature that the condition  $t \leq 2\delta$  or  $w \leq 2\delta$  is recommended, because it makes it possible to minimize the energy losses and to avoid the heating of the inductor. However, the changing of the width affects three parameters: the inter-turn distance, the external diameter and the internal diameter, which is why it is advised to take the condition  $t \leq 2\delta$  instead  $w \leq 2\delta$ .

In this study, we have shown through different numerical simulations that the thickness  $t \prec 2\delta$  generates more losses than the rejected condition  $t \succ 2\delta$  and  $t = 2\delta$  is best condition.

## 5.2. Choose of the optimal gap

The analysis of the obtained results will also allow us to choose the optimal gap.

The  $100\mu\text{m}$  gap generates the highest parasitic capacitance  $C_{\text{gap}}$  (Table III.5) in particular with the insertion of the Kapton and also generates the highest leakage current through the gap with and without kapton (figure III.17). So, the  $100\mu\text{m}$  gap is rejected.

The  $500\mu\text{m}$  and  $1000\mu\text{m}$  gaps shown very close results, therefore, to choose the optimal gap between the two, we must first study the electromagnetic and thermal effects (Chapter V).

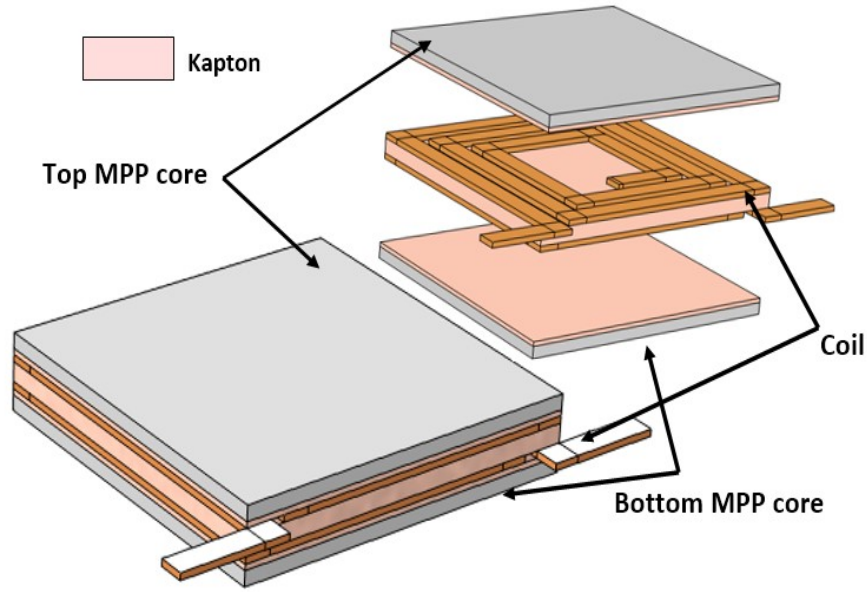
## 6. SIZING OF THE MAGNETIC CORE

The results analysis of table III.2 presenting the measured inductances values for different thicknesses and different gaps, we note that none of these values reached the inductance value calculated for the operation of the converter (chapter II, paragraph 4.2). To increase the value of the inductance to the desired value, we will insert a magnetic core in the dual-layer inductor.

The mainly role of the magnetic core in an inductor is to increase the strength of the magnetic field as well as the inductance value. The magnetic core which will be inserted in our dual-

layer inductor must meet two requirements of the converter: the value of the inductance necessary for its operation and the restricted volume.

The magnetic core will be in the form of two square layers placed on the top and bottom of the dual-layer inductor, as shown in figure III.20. Its volume will be determined according to the energy stored by this later.



**Figure III. 20:** The designed final form of the dual-layer inductor with a detailed view

The selection of magnetic material is critical and accurate since it relies on several key characteristics: resistance, degradation relevant to the applied frequency, and magnetic permeability. Referring to the literature [7-10], we have picked the Molypermalloy Powder (MPP). Molypermalloy Powder has a relative permeability of 60, it mainly comprises 2% molybdenum, 81% nickel, and 17% iron. Under DC and AC bias conditions, MPP offers high resistance, low hysteresis, negligible eddy current losses, and an excellent inductance stability. The saturation flux is approximately 8,000 Gauss (0.8 T).

### 6.1. Magnetic energy storage.

The maximum stored energy is determined from the inductance value of the inductor and the maximum current (Equation III.10).

$$W = \frac{1}{2} L I_{\max}^2 \quad \text{Equation (III.10)}$$

For an inductance value of 10μH and a maximum current  $I_{LMAX} = 7A$ , the maximum stored energy will be  $W = 245 \mu J$

## 6.2. Magnetic core volume

The dimensioning of the magnetic core (MPP) is based on the volume necessary to store the maximum amount of energy. We need to know the volume density of energy characterizing the MPP to calculate this volume. This density is given by expression III.11 [11-14]

$$W_{vmax} = \frac{B_{max}^2}{2\mu_0\mu_r} \text{ Equation (III.11)}$$

With a relative permeability  $\mu_r = 60$  and a saturation induction  $B_{max} = 0.8T$ , we will have:  $W_{vmax} = 4247 \text{ j / m}^3$ .

Relation III.12 allows to determine the volume of the MPP core required for a value of inductance  $L = 10 \mu H$

$$V = \frac{W}{W_{vmax}} \approx 60mm^3 \text{ Equation (III.12)}$$

15% added to the volume to cover all the losses energy caused by applying frequency and the temperature, especially since, this application is expected to be employed in a harsh environment. The magnetic core volume is divide into two equal flat layers with dimensions 10mm X 10mm X0.35mm]. A Kapton layer of 200μm is placed between the magnetic core and the inductor (Figure III-20). A silicon layer is used as an inductor's substrate to raise the resistance to reduce parasite flow and for a good heat dissipation [15].

### 6.2.1. The inductance of the dual-layer inductor with the magnetic core

Figure III.21 shows behaviour of the inductance according to the frequency, once, the MPP magnetic core is added. We notice that, the inductance value decreases when the frequency increases. This is due to energy losses related to the conductor and the magnetic core which increase with frequency. When the greatest conductor thickness and the greatest gap are associated, the inductance takes the smallest value and cancels beyond 800 KHz.

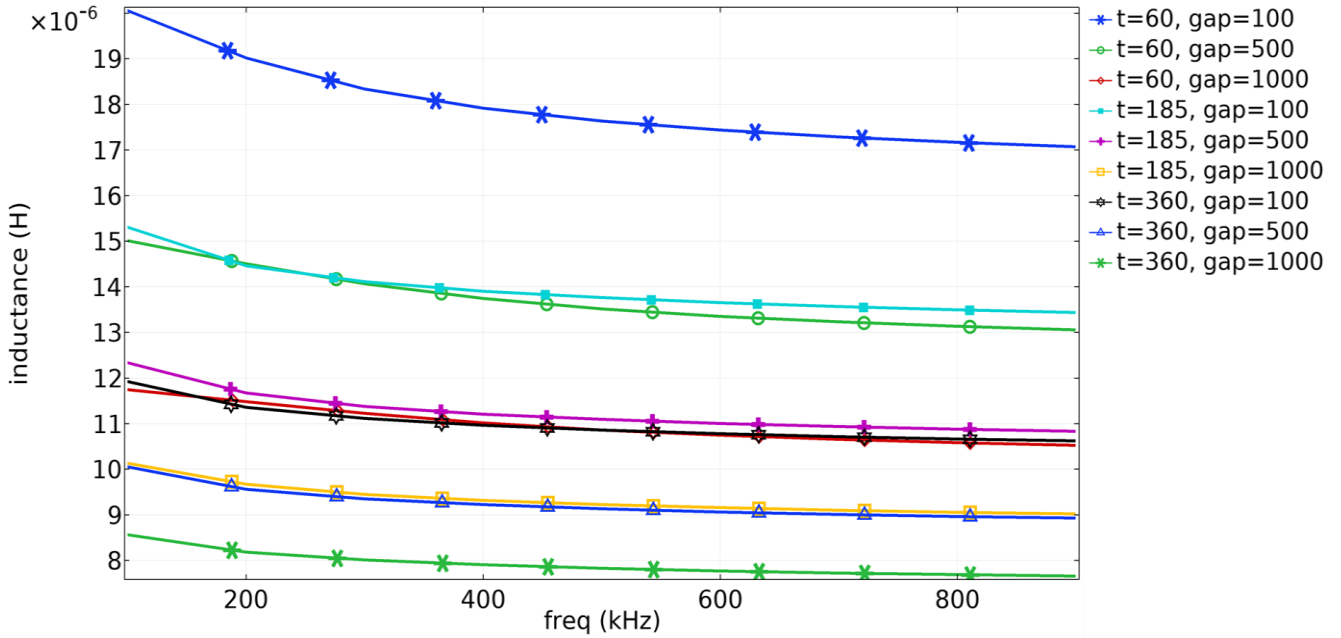
The numerical simulation results of table III.7 illustrate the inductance values for different thicknesses and gaps at DC and 500 KHz. The first observation made, is that the inductance value has been increased by the insertion of the magnetic core. So, our goal is achieved.



The highest inductance value is recorded for parameters (60/100). At 500KHz, parameters (185/500) and (360/100) give also a high inductance value compared to the others.

Gap Dg \ Thickness t	100μm		500μm		1000μm	
	DC	500KZ	DC	500Khz	DC	500Khz
60μm	$2.20 \times 10^{-5}$ H	$1.89 \times 10^{-5}$ H	$1.62 \times 10^{-5}$ H	$1.45 \times 10^{-5}$ H	$1.28 \times 10^{-5}$ H	$1.16 \times 10^{-5}$ H
185μm	$1.74 \times 10^{-5}$ H	$1.45 \times 10^{-5}$ H	$1.41 \times 10^{-5}$ H	$1.19 \times 10^{-5}$ H	$1.12 \times 10^{-5}$ H	$9.90 \times 10^{-6}$ H
360μm	$1.41 \times 10^{-5}$ H	$1.16 \times 10^{-5}$ H	$1.17 \times 10^{-5}$ H	$9.8 \times 10^{-6}$ H	$9.77 \times 10^{-6}$ H	$8.4 \times 10^{-6}$ H

**Table III. 7:** The inductance values with MPP core for different gap and thicknesses at DC and 500Khz



**Figure III. 21:** Frequency analysis of the inductance with MPP magnetic core for different gaps and thicknesses.

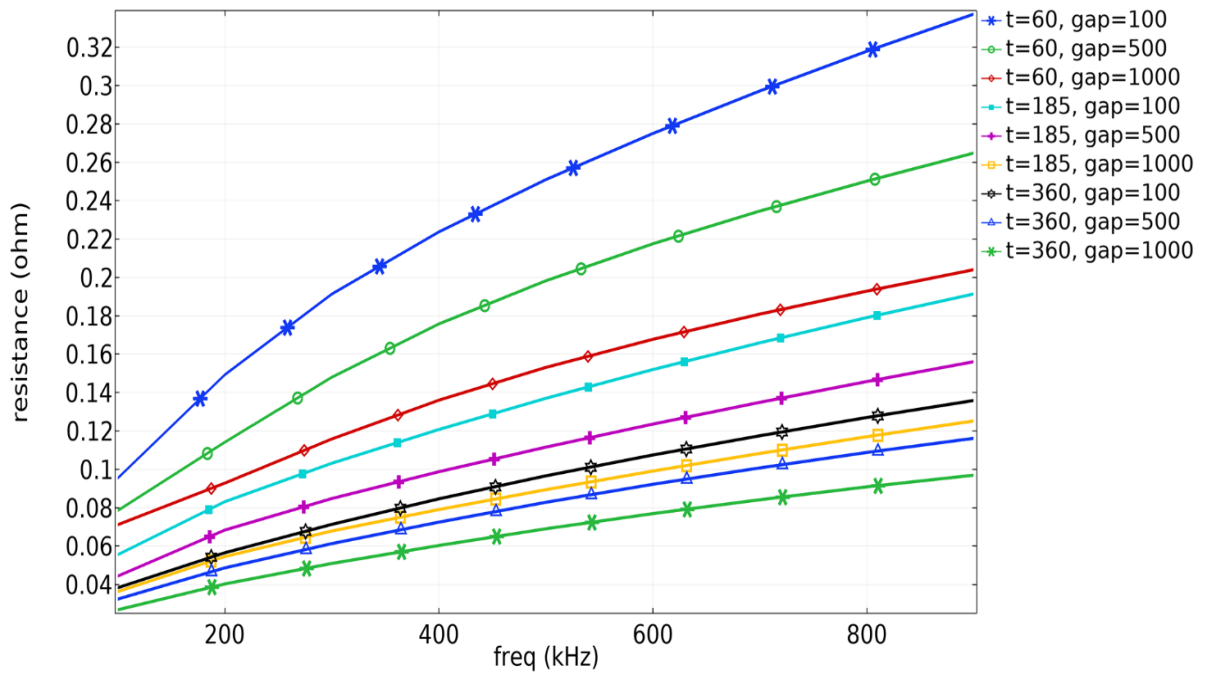
### 6.2.2. The resistance of the dual-layer inductor with magnetic core

The figure III.22 shows numerical frequency investigation of the series resistance for dual-layer inductor with different gap and thickness. The greatest resistance is recorded at 500KHz for inductor with parameters ( $t=60$  \_  $D_g=100$ ).

For more precision, we have grouped in table III.8 the measured values of series resistances at DC and 500 KHz for each case.

Gap Dg \ Thickness t	100μm		500μm		1000μm	
	DC	500KZ	DC	500Khz	DC	500Khz
60μm	0.0610Ω	0.251Ω	0.0198Ω	0.136Ω	0.0101Ω	0.096Ω
185μm	0.0612Ω	0.198Ω	0.0198Ω	0.111Ω	0.0101Ω	0.082Ω
360μm	0.0614Ω	0.153Ω	0.0199Ω	0.089Ω	0.0102Ω	0.068Ω

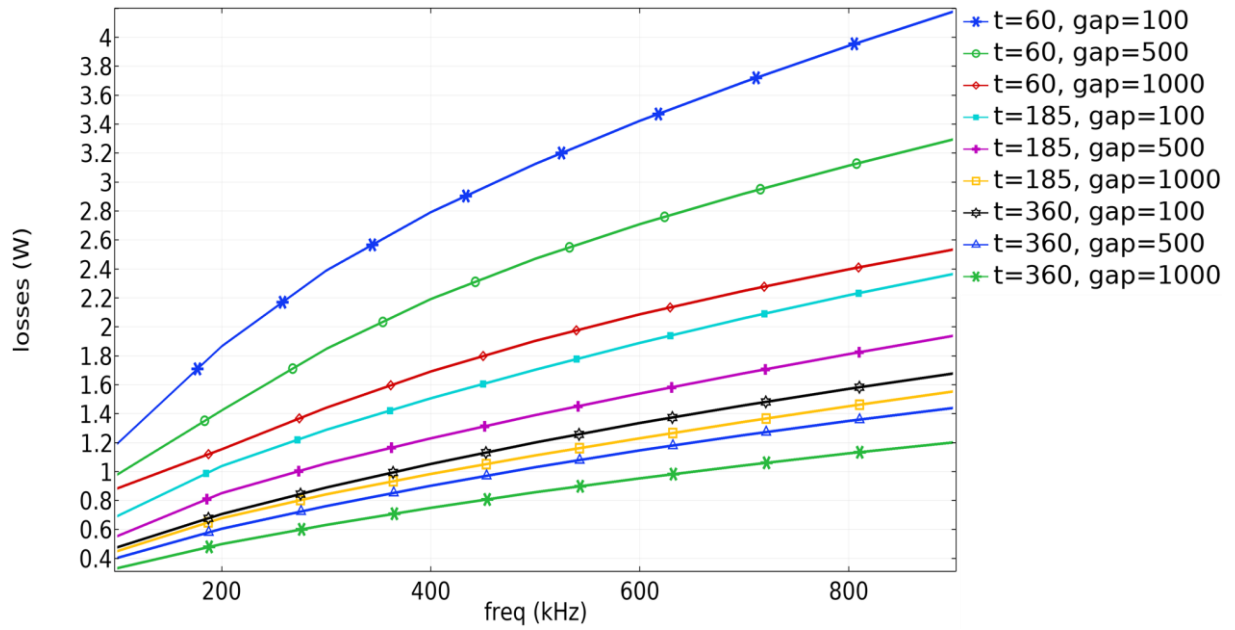
**Table III. 8:** Values of the series resistance of the dual layer inductor with MPP core at DC and 500Khz



**Figure III. 22:** Frequency analysis of the AC resistor of dual layer inductor with different gap and thicknesses

### 6.2.3. Losses investigation

Figures III.23 demonstrate the numerical simulation of AC losses results for the nine indicated cases using the finite element approach. A high-power loss is recorded for thin thicknesses inductor.



**Figure III. 23:** Variation of the AC losses according to the frequency with MPP core for different gap and thicknesses.

#### 6.2.4. The quality factors.

The analysis of figure III.24 indicates that all gaps associated to a very thin thickness of 60  $\mu\text{m}$  have the lowest quality factor, which could be explained by the high series resistance resulting from the small conductor section and the leakage current through the parasitic coupling capacitance between the two coils. Add to these disturbing effects, the non-uniform distribution of the current in the conductor caused by the applied frequency and the proximity effect. We conclude that inductors with too low a thickness are not recommended.

As it was mentioned previously, the thickness  $t=360\mu\text{m}$  is also rejected, because, it favours the skin effect.

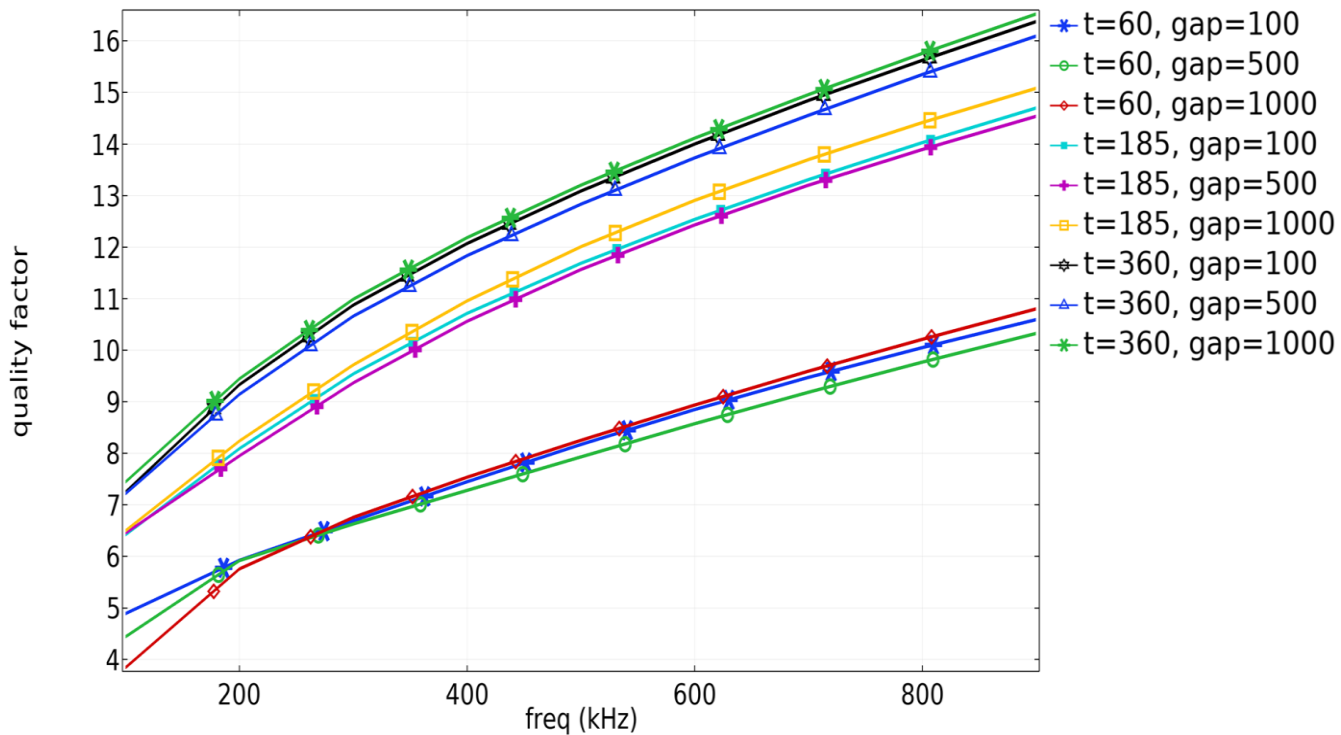
The results archived in table III.9 for the dual layer inductor with MPP at 500 KHz are extracted from figure III.24.

Gap Dg \ Thickness t	100 $\mu\text{m}$	500 $\mu\text{m}$	1000 $\mu\text{m}$
60 $\mu\text{m}$	8.17	7.93	8.25
185 $\mu\text{m}$	11.68	11.56	12.00
360 $\mu\text{m}$	13.08	12.83	13.19

**Table III. 9:** The quality factor of the dual layer inductor with MPP at 500 KHz

The gaps of 100 $\mu\text{m}$  and 1000 $\mu\text{m}$  associated with different thicknesses show slightly better-quality factors than that of 500 $\mu\text{m}$ . However, the 100  $\mu\text{m}$  gap generates a significant parasitic capacitance  $C_{\text{gap}}$  between the two coils (Table III.5) which favours significant leakage currents (Figure III.18). This gap is rejected.

The interpretation of all results presented in this 3rd chapter show very close results for the 500 $\mu\text{m}$  and 1000 $\mu\text{m}$  gaps. We will therefore leave the choice of the optimal gap after the study of the electromagnetic and thermal effects (Chapter V).



**Figure III. 24:** Variation of the quality factor according to the frequency for dual-layer inductor with MPP core for different gap and thicknesses.

## 7. THE VOLUME OCCUPIED BY THE DUAL-LAYER INDUCTOR

As the main object of this work is to reduce the size of the DC-DC power converter by reducing the size of its inductor, we present in table III.10 the volume occupied by the inductor for the different gaps and different thicknesses.

	60/100	60/500	60/1000	185/100	185/500	185/1000	360/100	360/500	360/1000
Volume (mm <sup>3</sup> )	132	172	222	157	197	247	192	232	282

**Table III. 10:** Presentation in mm<sup>3</sup> the volume of each inductor.

## 8. CONCLUSION

In this chapter we have established the designing and sizing of an integrated dual-layer planar inductor model for the DC-DC boost converter. Following several numerical simulations, we have been able to observe the behaviour of some important parameters (series resistance, quality factor, power losses, current density, inductance, leakage current). We concluded that these parameters need to be well studied, in order to implement an optimum design for the planar magnetics.

The study included nine different cases where it's shown that the gap and the conductor thickness have an important impact on the inductor's performance.

This study allowed us to conclude that:  $t = 2\delta$  is the optimum thickness of the conductor which gives the best results and minimizes energy losses.

Too small a gap promotes leakage currents between the two stacked coils and degrades the performance of the dual layer inductor. So very small gap is not recommended during the design of stacked inductors.

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# Chapter IV

Improvement of the Dual-layer Inductor and  
Design of a Corrector Block for the  
Converter Output Voltage

## 1. INTRODUCTION

In this chapter, our objective is to investigate the DC-DC boost converter's behaviour and performances containing each of the dual-layer inductors studied in the previous chapters.

In order to confirm the application and validate its well-functioning, first, we will design the electrical circuit of the dual-layer inductor. This technique is based on the physical derivation and circuit theory. Formulas are generated to calculate the technological parameters from the inductor layout [1-3].

Once the values of these parameters have been calculated, we will replace in the boost converter, the electric circuit of the ideal inductor by that of the dual-layer inductor, then, we simulate by PSIM software, the different waveforms of the currents and voltages of the inductor and the converter

In this chapter, we will, also present an approach allowing to design a smart converter which automatically adjusts its output voltage to the required voltage and keeps it stable whatever the input voltage coming from the PV module.

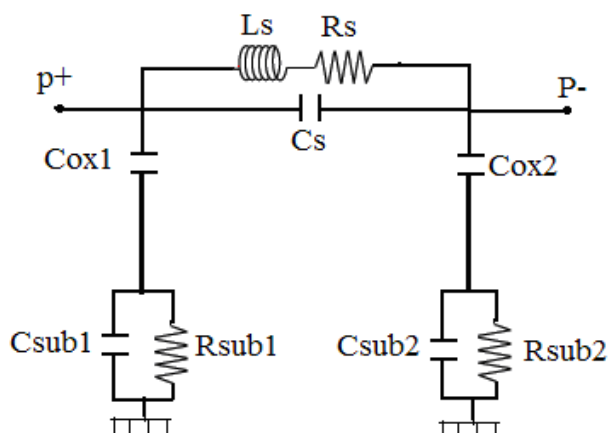
## 2. ELECTRICAL MODELLING

### 2.1. Electrical model of the coreless planar inductor

In 1990 Nguyen and Meyer [4] developed an integrated planar inductor on silicon using interconnection technology. They proposed a simple " $\pi$ " electrical model to describe the inductor's behaviour. An improved model was later developed by Ashby & al [5]. This model considers more physical mechanisms appearing in the inductor. The parameters of the improved model needed to be fitted from the experimental curves rather than having physical significance.

A few years later, Yue and Yong [9] reported a similar model (Figure IV-1) but with parameters more adapted to the geometry of the planar inductor. We will consider the square planar inductor and the model of Yue and Yong as a reference to discuss the important issues associated with such a device, including the serial inductance ( $L_s$ ), the serial resistor ( $R_s$ ) and the parasitic capacities ( $C_s$ ,  $C_{SUB1}$ ,  $C_{SUB2}$ ,  $C_{OX1}$ ,  $C_{OX2}$ ).





**Figure IV. 1:** "  $\pi$  " electric model of a planar spiral inductor developed by Yue and Yong [9]

## 2.2. Electrical model with magnetic core.

When inserting a core between the insulator and the substrate, the resistances  $R_{mag1}$  and  $R_{mag2}$  are added to the circuit of figure IV.1. These resistances present the losses by Joule effects in the magnetic core and oppose the passage of currents induced by capacitive effect [6]. Figure IV-2 represents the model of the planar spiral inductor with a magnetic core. It represents a symmetrical  $\pi$  circuit with two poles and the parameters:

$L_s$  : Inductance of the conductive spiral.

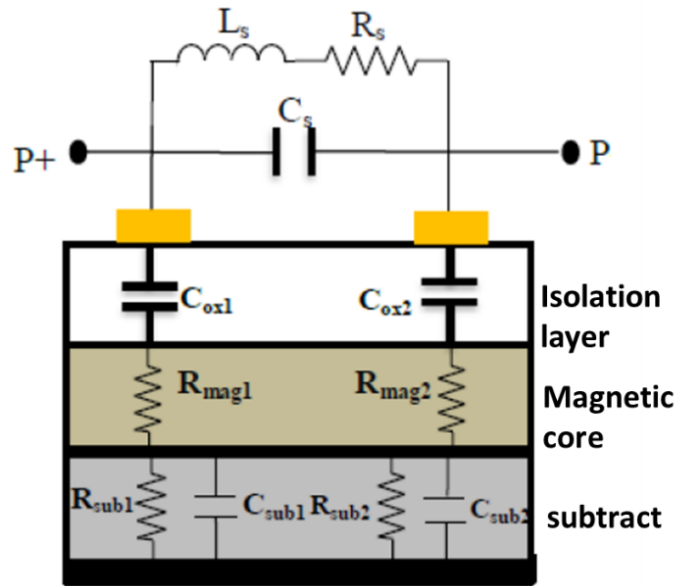
$R_s$ : The total series resistance of the conductor, composed of the continuous resistance  $R_{dc}$  depending on the resistivity of the material conductor and the resistance  $R_{ac}$  depending on the frequency characterizing the losses by skin effect.

$C_{ox}$ : Parasitic coupling capacity into the oxide.

$C_{sub}$ : Parasitic coupling capacity into the substrate.

$R_{sub}$ : Ohmic loss in the semi-conductive substrate.

$R_{mag}$ : Ohmic loss in the conductive magnetic core



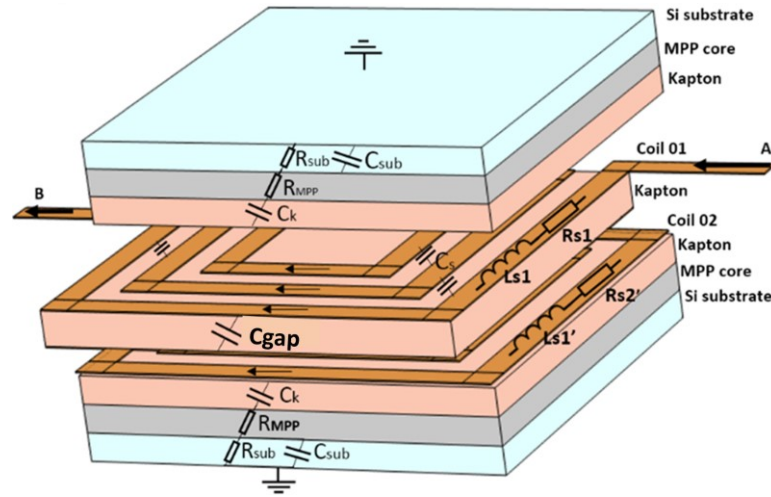
**Figure IV. 2:** Equivalent electrical circuit from the cross-section of a spiral planar inductor with magnetic core [6].

### 3. ELECTRICAL MODEL OF THE DUAL DUAL-LAYER INDUCTOR

The design of the equivalent circuit of the dual-layer inductor is an effective method to validate its good functioning in the application.

The advantage of this method exemplifies the ability to provide anticipation for the behaviour description of the inductor placed on the electrical circuit and maximum optimization of parasitic effects [7-8]. The form diagram of figure IV.3 presents every path possible of the current flow and the physical nature modelling for this passing (resistance, capacitance, or inducing).

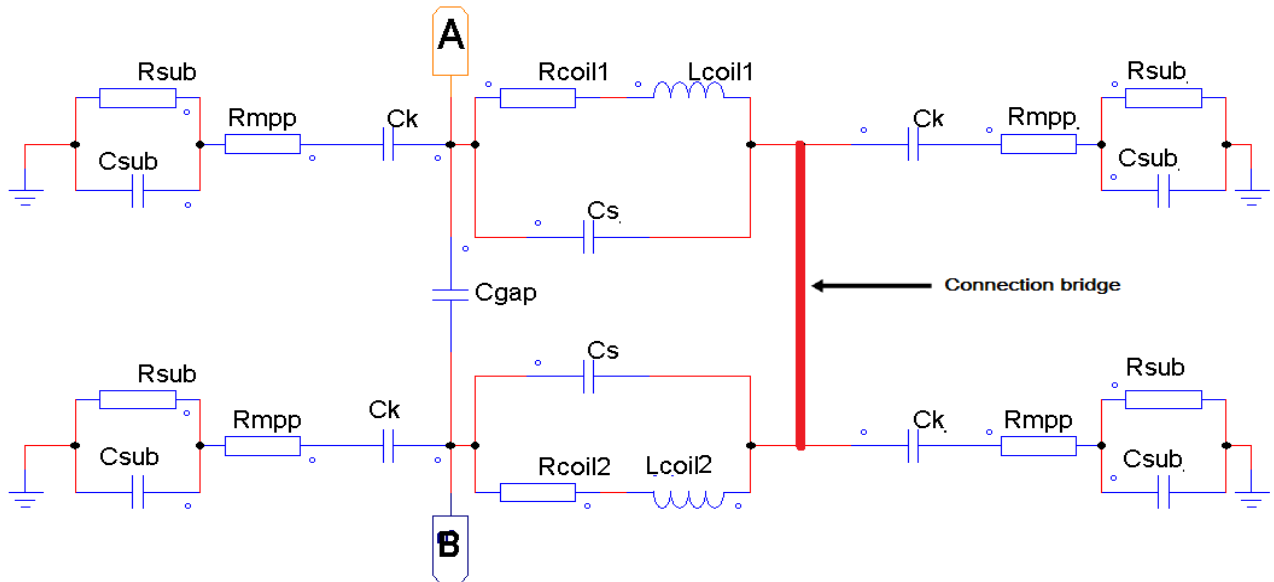
The equivalent circuit of the dual-layer inductor contains the inductances  $L_{s1}$ ,  $L_{s2}$  and the parasitic series resistances  $R_{s1}$  and  $R_{s2}$  which appears in each segment along the windings.  $C_{gap}$  the coupling capacitance between the two coils.  $C_k$ : the coupling parasitic capacitance between the conductive winding (conductor) and the magnetic core.  $R_{MPP}$  is the resistance associated with the magnetic layer,  $R_{sub}$  and  $C_{sub}$  are respectively the resistance and the capacitance related to the silicon substrate.



**Figure IV. 3:** 3D Final structure of dual-layer planar spiral inductor with parasitic elements illustration

We represent the diagram of figure IV.3 by its electrical equivalent model of figure IV. 4 in order to study the inductor's behaviour.

The equivalent circuit of the dual-layer inductor consists of two electrical models with a magnetic core (Figure IV.4) connected by a wire characterizing the connection bridge.  $C_{gap}$  is the parasite capacitor between the two stacked coils.



**Figure IV. 4:** Equivalent electrical circuit of the dual-layer inductor

## 4. THE TECHNOLOGICAL PARAMETERS OF THE DUAL-LAYER INDUCTOR

The realization of the dual-layer inductor was done after a smooth dimensioning of the geometric parameters and a good adjustment of the electrical parameters. Nevertheless, other elements must be taken into account to ensure that the results obtained favour the correct frequency behaviour of the component. To complete our work, we are going to study the various parasitic effects that may appear during the operation of dual-layer inductor in the boost application.

### 4.1. Calculation of parasitic capacitances ( $C_{gap}$ , $C_s$ , $C_k$ , $C_{sub}$ ).

The modelling of capacities in dual-layer inductors is done according to the concept of parallel plate capacities. In our model, we distinguish 4 types of capacities:

#### 4.1.1. Inter-spire capacitance $C_s$

The parasitic coupling capacitance between the turns  $C_s$  is expressed by relation (IV.1):

$$C_s = \varepsilon_0 \frac{t \cdot l_{avg}}{s} \quad \text{Equation (IV.1)}$$

Where:  $\varepsilon_0$  is the permittivity of the vacuum,  $t$  is the thickness of the conductor,  $L_{avg}$  is the average length of the spiral winding, and  $s$  is the inter-turns distance.

#### 4.1.2. Capacitance of the Kapton layer $C_k$

The insulating layer between copper and the MPP core generates a parasitic capacitance  $C_k$  which is due to the potential difference between these two conductors.  $C_k$  is calculated by expression IV.2.

$$C_k = \varepsilon_0 \varepsilon_k \frac{A_i}{t_k} \quad \text{Equation (IV.2)}$$

With  $\varepsilon_k$  is the relative permittivity of the insulating layer (Kapton),  $A_i$  is the section of winding layer in contact with the insulation ( $A_i = L_{avg} \times W$ ),  $t_k$  is the Kapton thickness.

#### 4.1.3. Capacitance of the substrate $C_{sub}$

The potential difference between the silicon layer junction and the ground expressed by the capacitor  $C_{sub}$  by equation IV.3

$$C_{sub} = \varepsilon_0 \varepsilon_{sub} \frac{A_i}{t_{sub}} \quad \text{Equation (IV. 2)}$$

Where:  $\varepsilon_{sub}$  is the relative permittivity of the silicon substrate,  $t_{sub}$  is the thickness of the silicon layer.

#### 4.1.4. The capacitance $C_{gap}$ between the two coils

We recall the expression IV.4 of  $C_{gap}$ , already calculated in chapter 3 paragraph 4.5.1.

$$C_{gap} = \varepsilon_0 \varepsilon_r \frac{A_i}{D_g} \quad \text{Equation (IV. 3)}$$

With  $\varepsilon_k$  is the relative permittivity of the insulating layer (Kapton) between coils.  $A_i$  is the interaction area between the top and bottom layers and  $D_g$  is the width of the gap.

### 4.2. Calculation of parasitic resistances ( $R_s$ , $R_{SUB}$ , $R_{MPP}$ ).

#### 4.2.1. The $R_s$ parasitic series resistance

The  $R_s$  series resistance that appears along the conductor is due to joules effects. In a dynamic regime, the copper conductor suffers from the effects of skin and proximity. In first approximation,  $R_s$  can be expressed from the resistivity of the conductor  $\rho$  and its average length  $L_{avg}$  by formula (IV.5):

$$R_{s1} = R_{s2} = \rho_{copper} \frac{l_{avg}}{t.w} \quad \text{Equation (IV. 4)}$$

Where  $\rho_{copper}$  is the Electrical resistivity of copper.

#### 4.2.2. The $R_{MPP}$ parasitic resistance of the magnetic core

$R_{MPP}$  magnetic core resistance represents ohmic losses in the Molypermalloy powder core and it's calculated from equation IV.6

$$R_{MPP} = \rho_{MPP} \frac{t_{MPP}}{A} \quad \text{Equation (IV. 5)}$$

Where  $t_{MPP}$  is the thickness of the magnetic core layer,  $\rho_{MPP}$  is the electrical material resistivity of the Molypermalloy powder core.

### 4.2.3. The $R_{sub}$ parasitic resistance of the substrate

$R_{sub}$  substrate resistance represents ohmic losses in the silicon layer and it's given by equation IV.7

$$R_{sub} = \rho_{sub} \frac{t_{sub}}{A} \quad \text{Equation (IV. 6)}$$

Where  $t_{sub}$  is the thickness of the silicon layer and  $\rho_{sub}$  is the electrical resistivity of silicon.

Where  $t_{sub}$  and  $\rho_{sub}$  are respectively, the thickness of the silicon layer and its electrical resistivity.

### 4.3. Assumption of symmetry

Because of the assumption of symmetry to the electric circuits shown in figures IV.2, the parasitic elements  $C_{sub}$ ,  $R_{sub}$ ,  $C_k$ , and  $R_{MPP}$  are divided into two equal parts and placed on each side of the poles. They are expressed by the following relationships:

$$C_{sub1} = C_{sub2} = \frac{C_{sub}}{2} \quad \text{Equation (IV. 7)}$$

$$R_{sub1} = R_{sub2} = 2R_{sub} \quad \text{Equation (IV. 8)}$$

$$C_{k1} = C_{k2} = \frac{C_k}{2} \quad \text{Equation (IV. 9)}$$

$$R_{MPP1} = R_{MPP2} = 2R_{MPP} \quad \text{Equation (IV.10)}$$

### 4.4. Material characteristics

To calculate the values of the electrical parameters, we use the geometrical dimensioning results, as well as the characteristic properties of the materials used in the manufacture of the dual-layer inductor (Table IV.1).

layers	Thickness ( $\mu\text{m}$ )	Relative permittivity $\epsilon_r$	Electrical resistivity ( $\Omega\cdot\text{m}$ )
Copper	60/185/360	/	1.7e-8
Kapton	200	3.85	
Molypermalloy	350	/	6e-7
Silicon(si)	100	11.8	18.5

**Table IV. 1:** The electrical properties of the materials utilized.

The calculation results of the technological parameters of the dimensioned dual-layer inductor are grouped in table (IV.2).

The electrical parameters	Calculated values
$Ck1=Ck2=Ck/2$	5,16E-12 F
$Csub1=Csub2=Csub/2$	3,16E-11 F
$Cs$ (60/185/360)	7,19E-14 F/ 2,21E-13 F/ 4,32E-13 F
$Cgap=Ck'$ (100/500/1000)	2,02E-11 F/ 4,04E-12 F/ 2,02E-12 F
$Rmpp1=Rmpp2=2Rmpp$	1,734195697 $\Omega$
$Rsub1=Rsub2=2Rsub$	1,53E+01 $\Omega$

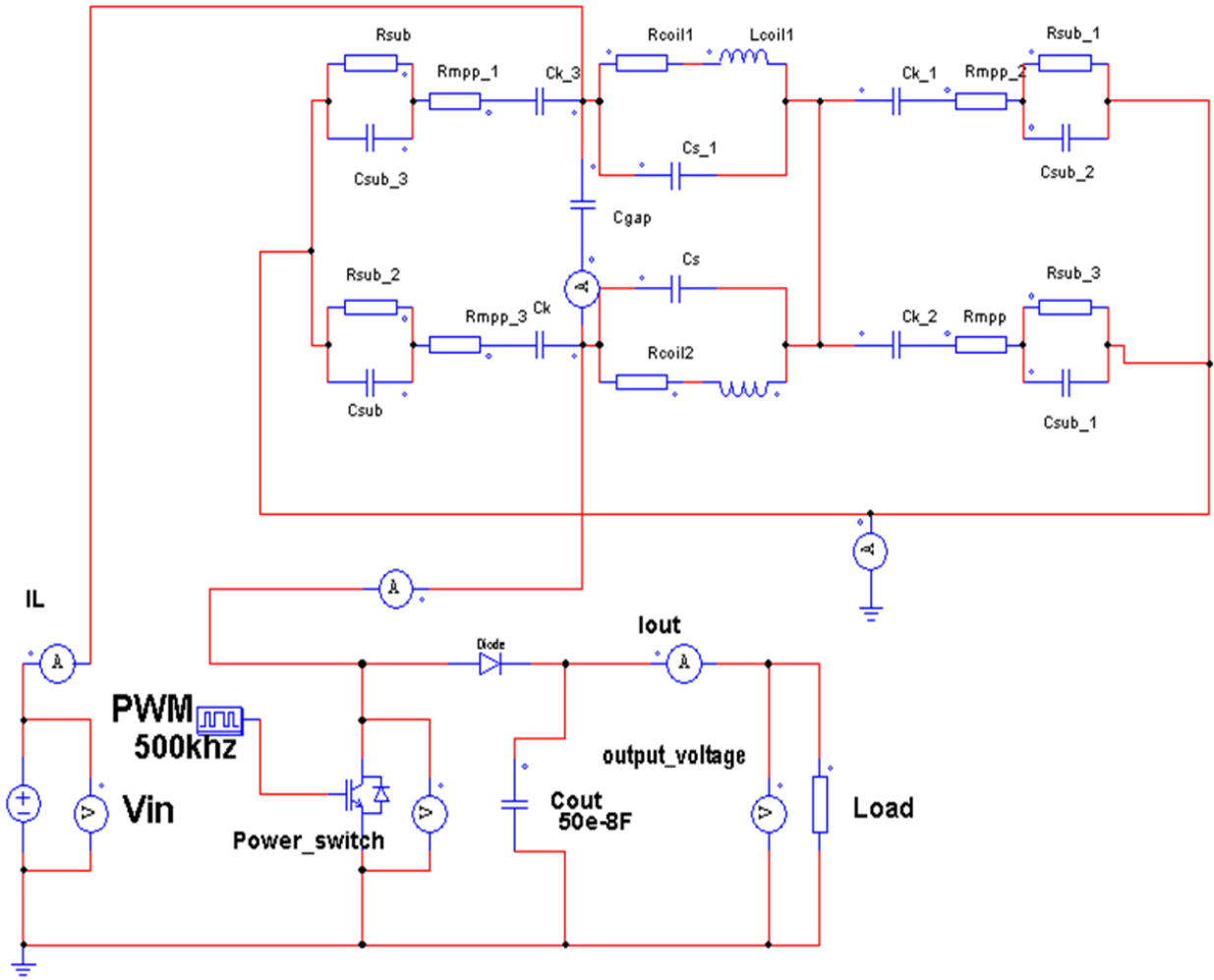
**Table IV. 2** The calculation results of the technological parameters

## 5. SIMULATION OF THE DC-DC BOOST CONVERTER WITH THE EQUIVALENT CIRCUIT OF THE DUAL-LAYER INDUCTOR.

To validate the proper functioning of our inductors models and to ensure that the geometric dimensioning is correctly carried out and that the parasitic effects resulting from the integration are strongly attenuated, we use the PSIM simulation software. 9.0.3.

We simulate, at first, the output voltage wave form of the DC-DC boost converter containing the 9 different circuit of the dual-layer inductor.

The electrical schematic of the DC-DC boost converter with the equivalent circuit of the dual-layer inductor is shown in Figure IV.5,



**Figure IV. 5:** The electrical schematic of the DC-DC boost converter containing the equivalent circuit of the dual-layer inductor

### 5.1. Simulation results

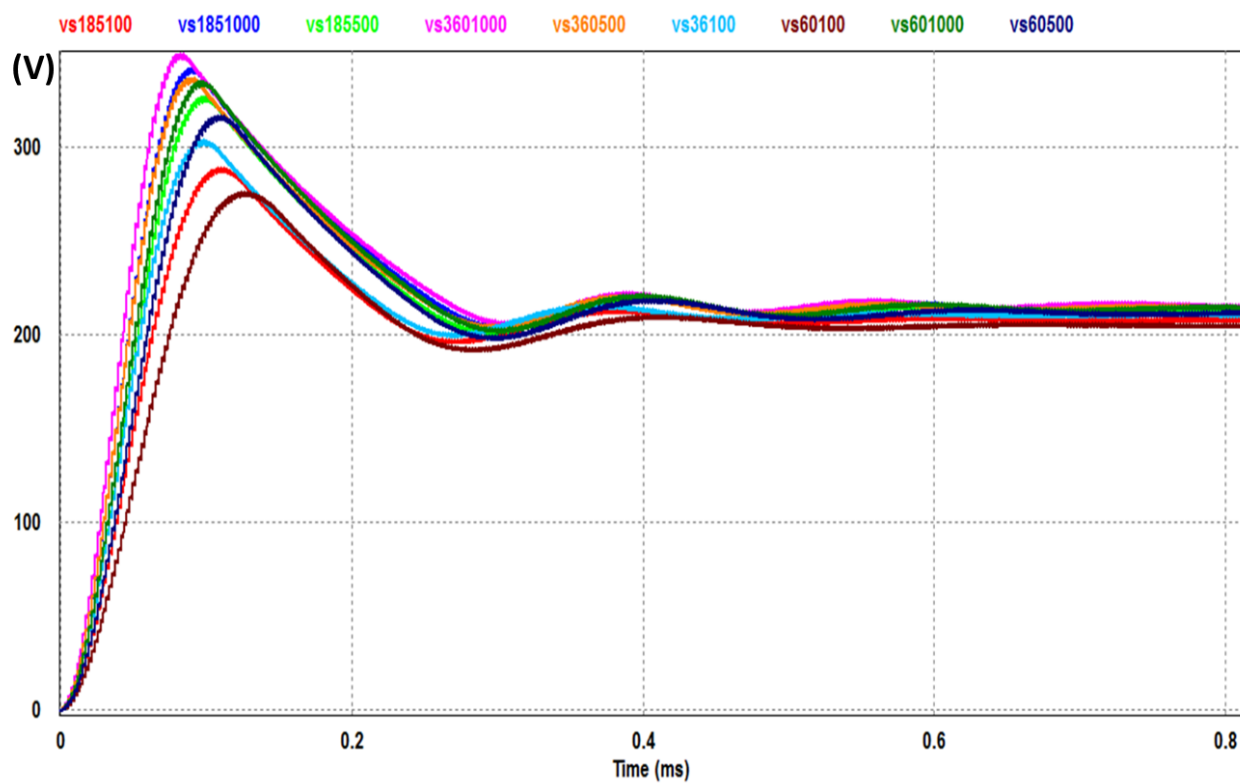
The electrical simulation has been done by replacing the ideal inductor of figure II.4 by the equivalent circuit of the dual-layer inductor. The simulation for the nine cases was done with the same duty cycle calculated in chapter II, paragraph 4.1.

Figure IV.6 presents the output voltage waveform of the DC-DC boost power converter with the equivalent circuit of the dual layer inductor. The output voltage is simulated for each pair (thickness, gap).

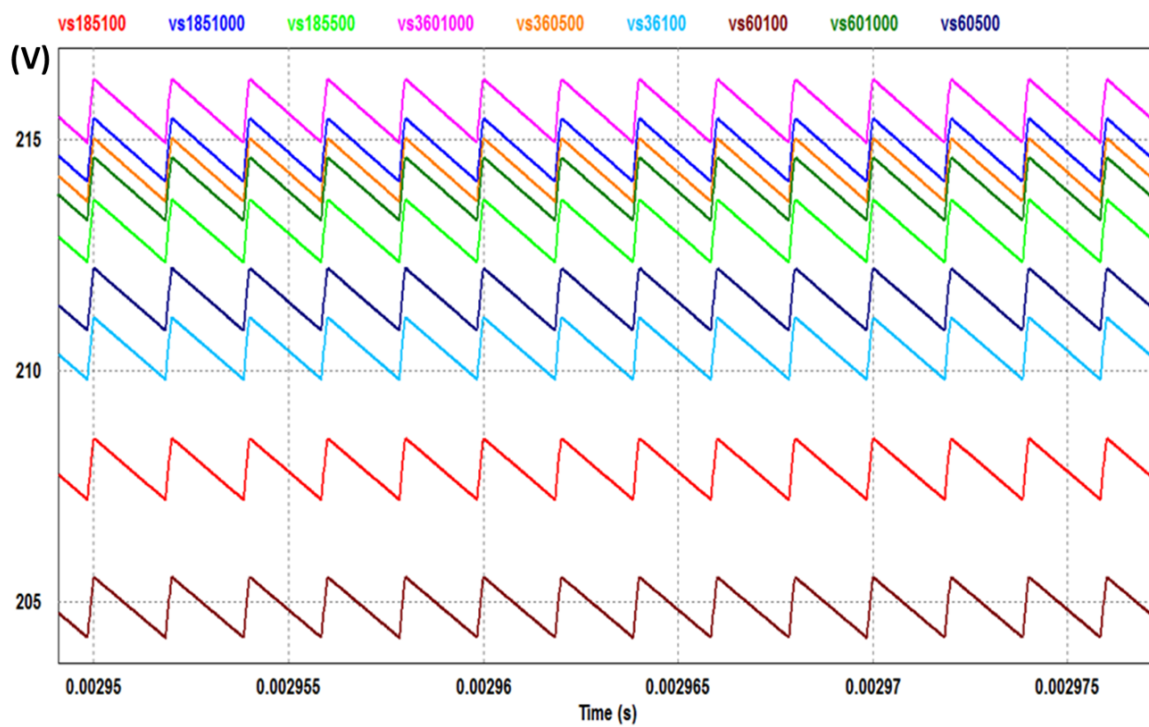
Figure IV.7 shows a close view of the outputs voltages with their ripples.

The average values of the outputs voltages of figure IV.7 are gathered in table IV.3.





**Figure IV. 6:** The output voltage waveform of the boost converter containing the dual-layer inductor



**Figure IV. 7:** The Ripples of the different output voltages

Inductor(thickness/gap)	Output Voltage
60/100	204.50V
60/500	211.70V
60/1000	214.40V
185/100	207.70V
185/500	212.81V
185/1000	214.38V
360/100	210.53V
360/500	214.89V
360/1000	216.40V

**Table IV. 3:** The measured output voltage average values for the nine cases

## 5.2. Interpretation of the results

According to the electrical simulation, we observe that the average output voltages displayed by table IV.3 are lower than the desired voltage 220V. This drop is due to parasite elements and the inductance value that differs for each case.

We notice that inductors with the thinnest winding display lower output voltage compared to the larger windings. This behavior indicates that the conductor thickness affects the output voltage. So, we conclude that a thickness  $t \prec 2\delta$  is not recommended.

We also notice that inductors with the smallest gap show the lowest output voltage. This is due to the leakage currents which increase between the two stacked coils when the gap is very thin. We also, conclude that the gap affects the output voltage and a thin gap is not recommended.

## 6. CORRECTION OF THE OUTPUT VOLTAGE

The correction of the output voltage will be done by the correction of the duty cycle. The output voltage of a DC / DC boost is obviously related to the duty cycle, hence any change in the duty cycle leads to a change in the output voltage. As a result, we can keep the output voltage fixed by assigning a duty cycle for each of the nine cases.

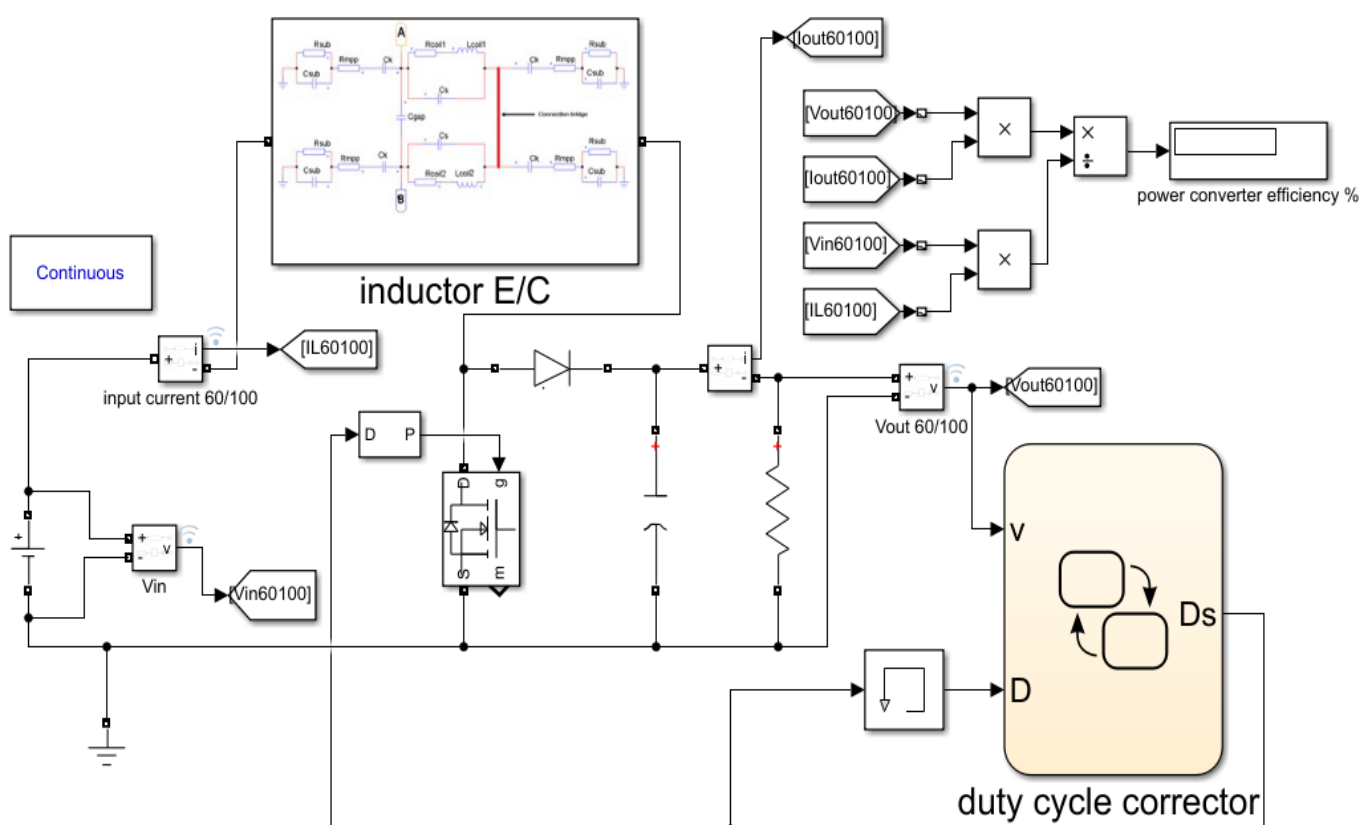
On this principle, we realized a control logic on MATLAB Simulink based on the Stateflow diagram presented in figure IV.9 in order to sort the appropriate duty cycle to adjust the output voltage to 220V according to the received input voltage. The operation of this logical control is based on direct supervision of the converter output. If the output voltage is lower or higher

than the desired voltage (220V), the algorithm enters a loop that adjusts the duty cycle with a variable step until the desired voltage is reached.

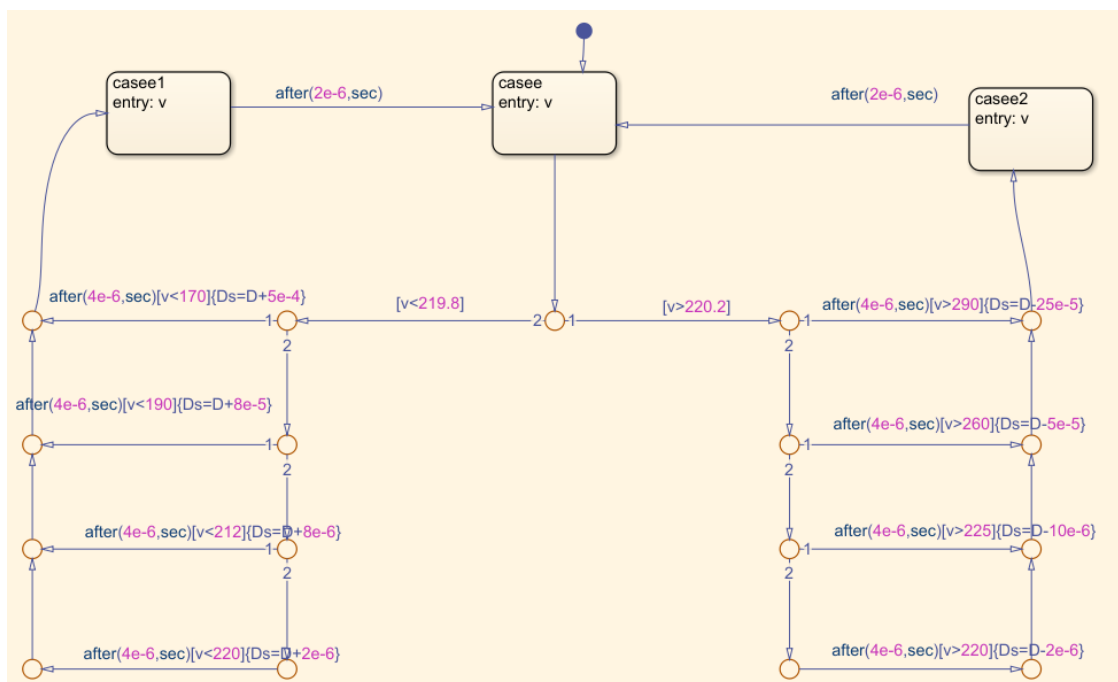
The variation of the step is different because it depends on the output voltage. The step is great for the outputs lower than the wished voltage and it's small steps for high output voltages. The block corrector avoids the waving behavior of the output voltage and shows a great precision and control.

The electrical simulation shows an excellent control and fast correction of the duty cycle. This method could take the supervision of the output voltage of the DC-DC boost converter in a photovoltaic system. Knowing that the Collapse of the output voltage in a PV system could be caused by the changes in material properties due to several factors such as, temperature, shading, and humidity. So, we can say that, the design of this system has a very beneficial contribution for photovoltaic systems.

Figure IV.8 shows the electrical schematic of the DC-DC boost converter in Matlab /Simulink, also shows the duty cycle Stateflow block and the equivalent circuit for the inductor.



**Figure IV. 8:** MATLAB Simulink circuit of the DC-DC boost converter including the equivalent circuit of the inductor and the duty cycle corrector block.



**Figure IV. 9:** The DC-DC boost duty cycle corrector Stateflow model

## 7. RESULTS AFTER DUTY CYCLE CORRECTION

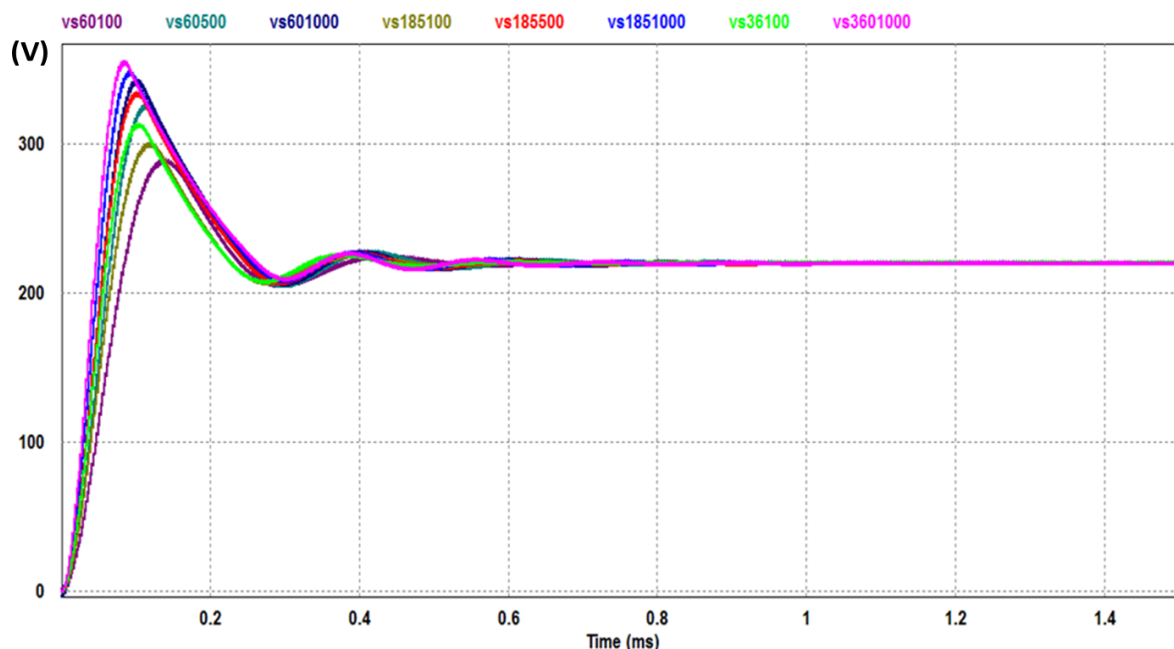
For all circumstances, the electrical simulation of the DC-DC boost converter utilizing the equivalent circuit of the dual-layer inductors reveals that the output voltage is exactly as required (220V). This means that the proposed method was effective in adjusting the output as needed by providing the proper duty cycle for each case.

Table IV.4 presents the new duty cycle resulted from the electrical stimulation.

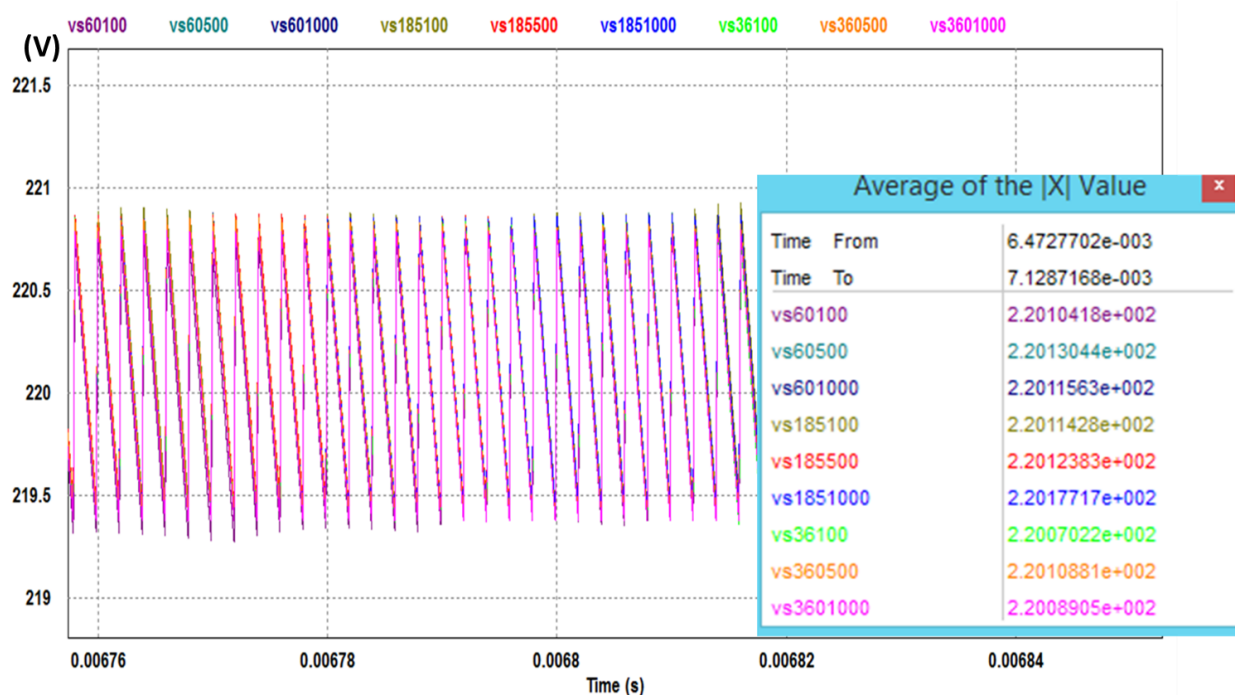
(thickness/gap)	Proper duty cycle %
<b>60/100</b>	90.40%
<b>60/500</b>	90.11%
<b>60/1000</b>	90.01%
<b>185/100</b>	90.27%
<b>185/500</b>	90.05%
<b>1850/1000</b>	89.97%
<b>360/100</b>	90.15%
<b>360/500</b>	90.00%
<b>360/1000</b>	89.95%

**Table IV. 4:** The new duty cycle for each case after correction

Figures IV.10 and III.11 show the output voltage waveform of the DC-DC boost converter for the nine cases, where we can see that in steady state, the out voltage is equal to 220 for all cases. We also see that the nine cases adopt the same behavior in the transition regime with different peak values.



**Figure IV. 10 :** The DC-DC boost converter output voltage wave form of each case  
(After correction)



**Figure IV. 11:** Zoom of the output voltage after correction

Figure IV.11 shows the nine output voltages well superimposed.

Table IV.5 displays the output voltage's peak values determined by the electrical simulation at the transitional regime. We see the greatest peak values recorded for the greater thicknesses. It is the same for the gaps.

The pairs (thickness, gap)	Maximum value of transitional regime
<b>60/100</b>	289.91V
<b>60/500</b>	327.00V
<b>60/1000</b>	343.59V
<b>185/100</b>	300.84V
<b>185/500/</b>	334.10V
<b>185/1000</b>	349.03V
<b>360/100</b>	314.10V
<b>360/500</b>	344.14V
<b>360/1000</b>	356.06V

**Table IV. 5:** The peak output voltage value recorded at transitional regime

## 8. THE OUTPUT RIPPLES

After correcting the output voltage, we measured the ripples  $\Delta V_{out}$  for each of the nine cases (Table IV.6). These results are derived from simulations of their equivalent electrical circuits containing the corrector block.

We observe that for all cases, the  $\Delta V_{out}$  didn't exceed the 0.7%  $V_{out}$ . This value is lower than that required by the specifications.

inductors	$\Delta V_{out}$
<b>60/100</b>	1.424 V
<b>60/500</b>	1.419 V
<b>60/1000</b>	1.437 V
<b>185/100</b>	1.422 V
<b>185/500</b>	1.479 V
<b>185/1000</b>	1.490 V
<b>360/100</b>	1.423 V
<b>360/500</b>	1.407 V
<b>360/1000</b>	1.414 V

**Table IV. 6:** The output voltage ripples for each case (after correction).

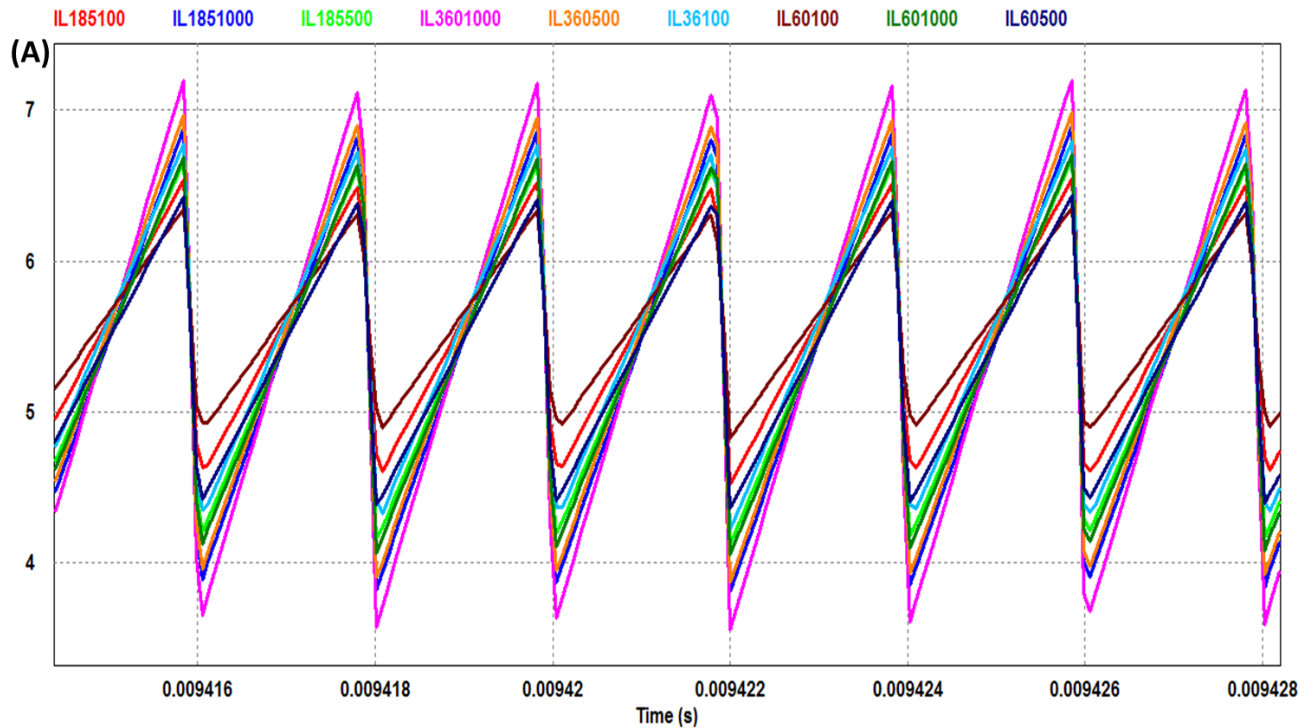
## 9. THE FLOWING CURRENT IN THE INDUCTOR

Figure IV.12 depicts the waveform of the currents flowing in the dual-layer inductor for each case. The results of the electrical simulation have been gathered in table IV.7.

We observe that the inductors with small gaps have a low current ripple, which is generally explained by the high inductance value. Usually, in boost converter, the inductance is inversely proportional to the current ripple. This relation is confirmed by equation IV.12.

$$\Delta I_L = \frac{V_{in} \times D}{f \times L} \quad \text{Equation (III. 11)}$$

We also notice that for the three different gaps, the smallest ripples are attributed to the thinnest conductor thickness.



**Figure IV. 12:** The wave form of the inductor current for each case

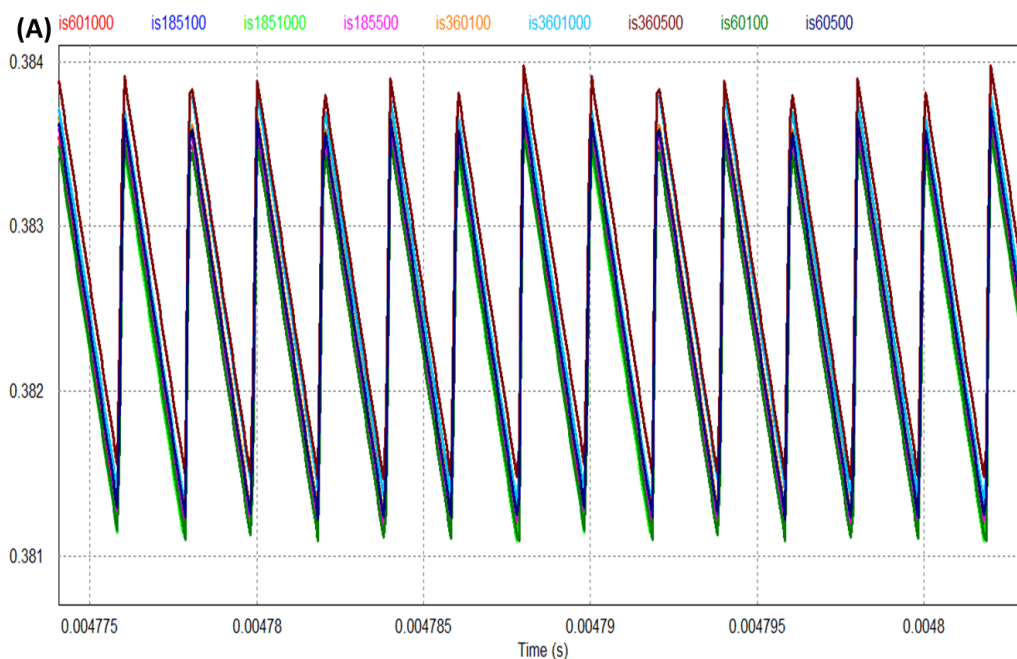
Inductors	ILavg	ILmax	ILmin	$\Delta IL$
<b>60/100</b>	5.55 A	6.30 A	4.82 A	1.47 A
<b>60/500</b>	5.41 A	6.41 A	4.41 A	2.00 A
<b>60/1000</b>	5.38 A	6.67 A	4.10 A	2.56 A
<b>185/100</b>	5.56 A	6.52 A	4.63 A	1.88 A
<b>185/500</b>	5.41 A	6.64 A	4.18 A	2.45 A
<b>185/1000</b>	5.36 A	6.86 A	3.86 A	2.99 A
<b>360/100</b>	5.56 A	6.76 A	4.36 A	2.39 A
<b>360/500</b>	5.44 A	6.95 A	3.94 A	3.00 A
<b>360/1000</b>	5.40 A	7.17 A	3.63 A	3.54 A

**Table IV. 7:** The flowing current in the inductor for each case (after correction)

## 10. THE OUTPUT CURRENTS

The waveform of the output current resulting from the electrical stimulation is presented by figure IV.13 for the different cases. We find that there is no significant difference; the nine curves are almost superimposed.

The minimum, maximum and average values of the output current, as well as the ripples are grouped in table IV.8



**Figure IV. 13:** The output current waveform for each case (after correction)



inductors	Iout_avg	Iout_max	Iout_min	Δout_I
<b>60/100</b>	38.23e-2 A	38.35e-2 A	38.11e-2A	0.24 e-2A
<b>60/500</b>	38.23e-2 A	38.36e-2 A	38.11e-2A	0.24 e-2A
<b>60/1000</b>	38.23e-2 A	38.35e-2 A	38.11e-2A	0.24 e-2A
<b>185/100</b>	38.24e-2 A	38.36e-2 A	38.12e-2A	0.24 e-2A
<b>185/500</b>	38.24e-2 A	38.36e-2 A	38.12e-2A	0.24 e-2A
<b>185/1000</b>	38.24e-2 A	38.36e-2 A	38.12e-2A	0.24 e-2A
<b>360/100</b>	38.26e-2 A	38.38e-2 A	38.14e-2A	0.24 e-2A
<b>360/500</b>	38.26e-2 A	38.38e-2 A	38.14e-2A	0.24 e-2A
<b>360/1000</b>	38.26e-2 A	38.38e-2 A	38.14e-2A	0.24 e-2A

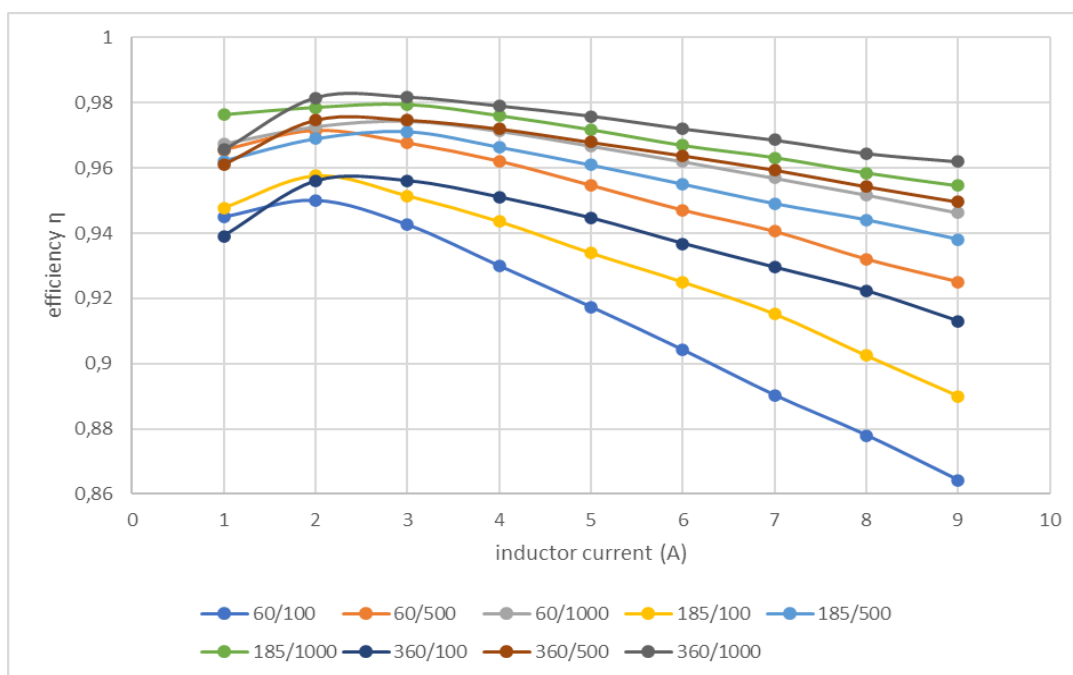
**Table IV. 8:** The resulted data of the output current for each case after correction

## 11. THE EFFICIENCY OF THE CONVERTER

A DC-DC boost power converter's efficiency is determined by comparing its input power to its output power. The theoretical efficiency of a boost converter is equal to 1. It is the ratio between its output power ( $P_{out}$ ) and its input power ( $P_{in}$ ), as presented in equation IV.13.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \quad \text{Equation (IV. 12)}$$

In order to investigate the converter efficiency, we have run out an electrical simulation based on the variation of the load resistance value. This simulation made it possible to observe the variation of the power converter efficiency according to the current flowing in the dual-layer inductor (Figure IV.14). We have grouped in table IV.9 the efficiency values measured for an average current of 5A taken from the specifications of the converter.



**Figure IV. 14:** Presentation of the power converter efficiency for different inductors.

binomials (thickness, gap)	Efficiency % (5A)
60/100	91,74%
60/500	95,46%
60/1000	96,68%
185/100	93,39%
185/500	96,09%
185/1000	97,17%
360/100	94,46%
360/500	96,79%
360/1000	97,59%

**Table IV. 9:** The efficiency values measured for an average current of 5A

We observe in figure IV.14, that the efficiency is better for low currents and when, the current increases, the efficiency decreases almost linearly.

Table IV.9 shows that converter including inductor with thin gap presents the lowest efficacy, because, of the important leakage currents. We also, notice that the lowest efficiency is recorded for the most thin conductor thickness because of its low-quality factor.

## 12. CONCLUSION

Chapter IV was devoted to the electrical modelling of the dual-layer inductor with different thicknesses and gaps in order to integrate it into our boost DC-DC converter. Nine dual-layer inductors with different conductor thicknesses and different gaps have been studied in this chapter.

The extraction of the technological parameters allowed us to design the electrical circuit of the dual-layer inductor. Using the PSIM simulation software, we have visualized the output voltage of the boost converter as well as the current flowing in the inductor with different thicknesses and different gaps. The voltage assigned to the smallest thickness has presented the worst result compared to the other thicknesses; the same is true for the smallest gap.

Following these results, we have concluded that too narrow gap and a very thin thickness are not recommended for the stacked planar inductors.

We have noticed in our results that, the values of the output voltages measured for the nine cases were lower than the desired value (220V). To correct this defect, we have connected to the boost converter, the designed corrector block. The carried-out simulations have shown perfect results.

These simulations allowed us to validate the proper functioning of the corrector block and the boost converter.

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# Chapter V

## Magnetothermal Behaviour of the Dual-layer Inductor

## **1. INTRODUCTION**

The study of electromagnetic and thermal behaviour is an essential operation in designing integrated passive components, because the reduction in volume leads to many problems that need to be resolved to guarantee the proper functioning and reliability of the component. The problems encountered during the volume reduction are manifested by an intense magnetic flux that can saturate the core of the magnetic component, or parasitic currents increasing the temperature of the component and degrading its performance.

There is also the problem of heat dissipation which are of great importance. The thermal effects can manifest themselves in different ways, either by a temperature drift of the components, which leads to significant variations in their electrical performances, or by an increase in temperature, which can lead to a change in the state of the materials used in the component manufacturing, as well as many other problems. So, the electromagnetic and thermal study supports adequate sizing for the design of an electronic component.

The numerical simulation is a valuable tool for better understand electromagnetic and thermal behaviour. The COMSOL Multiphysics numerical software program was employed in this study.

## **2. ELECTROMAGNETIC AND THERMAL STUDY OF THE DUAL-LAYER INDUCTOR**

The physical modelling of the dual-layer inductor requires solving electromagnetic equations. In the literature, we often find these equations' numerical analysis methods, but some don't apply to spiral planar inductors because of the non-homogeneous medium surrounding these inducers[1-2].

The magnetothermal study of the dual-layer inductor is made by the COMSOL Multiphysics software. This step presents an essential operation in the design of the planar inductors, because it ensures adequate sizing for the design and practical implementation of an integrated inductor.

The electromagnetic study aims to visualize all the magnetic and electrical effects occurring during the operation of the inductor, such as: the distribution of the magnetic field lines, the current density distribution inside the conductor and the electric potential.

The thermal part consists of visualizing the temperature distribution in the different layers of the dual-layer inductor: conductor, core, and substrate. The numerical simulation results represent a powerful tool that better understands the magnetothermal behaviour and validates the geometrical and electrical parameters of the dimensioned inductor.

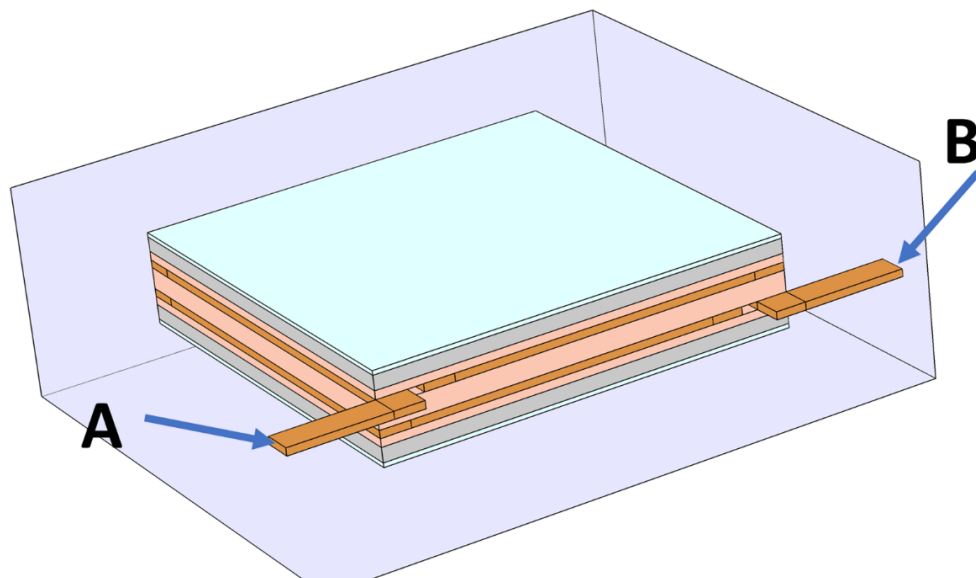
The simulation by COMSOL Multiphysics software requires two important steps: the introduction of the model geometry as well as its dimensions (the physical model) and the choice of materials used for design, because this software requires data that characterize the magnetic, thermal, and electric properties of these materials.

Our dual-layer inductor is composed of a copper spiral winding, a silicon substrate that promotes the evacuation of the thermal flow, an MPP magnetic core to channel the magnetic field lines and increase the value of the inductance. and an insulating layer of Kapton

### 2.1. The physical model

Figure V.1 presents the physical model of the dual-layer inductor, whose stages of design and sizing are presented in Chapters II and III. The study covers the influence of the conductor thickness and the gap on the electromagnetic and thermal behaviour of the dual-layer inductor.

Input current is indicated by A and the output by B, the initial current is 5 A and the input voltage is 17V with 500KHz operating frequency.



**Figure V. 1:** The Physical model of the dual-layer inductor

## 2.2. Mathematical model

The simulation results, obtained by the resolution of Maxwell equations (equations V.1) from which the mathematical model follows, allow to visualize the magnetic field lines, the electric potential and the distribution of the electric current density, The resolution process gives the solutions to the chosen operating frequency. The resolution of mathematical equations in COMSOL is carried out by the finite element method [3-6].

$$\begin{aligned}
 \nabla \vec{J} &= 0 \\
 \nabla \times \vec{A} &= \vec{B} \\
 \nabla \times \vec{H} &= \vec{J} \\
 \vec{J} &= \sigma \vec{E} + j\omega \vec{D} \\
 \vec{B} &= \mu_0 \mu_r \vec{H} \\
 \vec{D} &= \epsilon_0 \epsilon_1 \vec{E}
 \end{aligned}
 \tag{Equations (V.1)}$$

Where :

$\vec{H}$  : Magnetic field [A/m]

$\vec{B}$  : Magnetic flux density [T]

$\vec{J}$  : Electric current density [A/m<sup>2</sup>]

$\vec{A}$  : Magnetic vector potential [Wb/m]

$\vec{E}$  : Electric field [V/m]

$\vec{D}$  : Norm of electric displacement field [c/m<sup>2</sup>]

In 3D equations V.1 becomes.

$$\begin{aligned}
 \vec{J} &= J_x \vec{i} + J_y \vec{j} + J_z \vec{k} \\
 \vec{A} &= A_x \vec{i} + A_y \vec{j} + A_z \vec{k} \\
 \vec{H} &= H_x \vec{i} + H_y \vec{j} + H_z \vec{k} \\
 \vec{B} &= B_x \vec{i} + B_y \vec{j} + B_z \vec{k} \\
 \vec{E} &= E_x \vec{i} + E_y \vec{j} + E_z \vec{k}
 \end{aligned}
 \tag{Equations (V. 2)}$$

Also

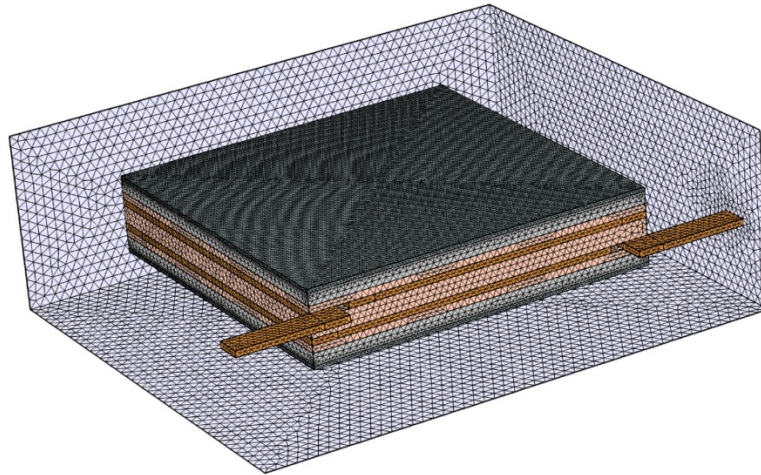
$$\begin{aligned} \frac{\partial J_x}{\partial x} + \frac{\partial J_y}{\partial y} + \frac{\partial J_z}{\partial z} &= 0 \\ \left( \frac{\partial A_z}{\partial y} - \frac{\partial A_y}{\partial z} \right) \vec{i} - \left( \frac{\partial A_z}{\partial x} - \frac{\partial A_x}{\partial z} \right) \vec{j} + \left( \frac{\partial A_y}{\partial x} - \frac{\partial A_x}{\partial y} \right) \vec{k} &= B_x \vec{i} + B_y \vec{j} + B_z \vec{k} \\ \left( \frac{\partial H_z}{\partial y} - \frac{\partial A_y}{\partial z} \right) \vec{i} - \left( \frac{\partial H_z}{\partial x} - \frac{\partial H_x}{\partial z} \right) \vec{j} + \left( \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} \right) \vec{k} &= J_x \vec{i} + J_y \vec{j} + J_z \vec{k} \quad \text{Equations (V.3)} \\ E_x \vec{i} + E_y \vec{j} + E_z \vec{k} &= -\frac{\partial V}{\partial x} \vec{i} - \frac{\partial V}{\partial y} \vec{j} - \frac{\partial V}{\partial z} \vec{k} \\ J_x \vec{i} + J_y \vec{j} + J_z \vec{k} &= \sigma(E_x \vec{i} + E_y \vec{j} + E_z \vec{k}) \end{aligned}$$

These equations are valid for all the configurations studied. As a result, we will only present physical models and border conditions specific to each case.

### 2.3. The mesh and the boundary conditions

#### 2.3.1. The mesh of the domain

The mesh principle consists of cutting the geometrical model into several triangles see figure V.2. The finer the mesh, the more precise the calculation results, however, the calculation time becomes more important, and the data size will be more significant.



**Figure V. 2 :** The mesh of the dual-layer inductor with MPP magnetic core  
in the study domain

### 2.4. The boundary conditions

The limits conditions on the boundaries of the study domain, indicated in Figure IV.3 are:

$$\vec{n} \cdot \vec{A} = 0 \quad \text{Equation (V.4)}$$

$\vec{n}$  is the vector normal to the boundary?



In 3D equation V.4 becomes

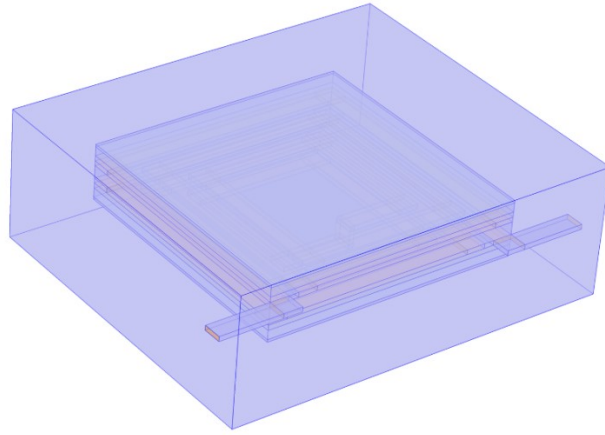
$$\begin{aligned} n_x \mathcal{A}_x + n_y \mathcal{A}_y + n_z \mathcal{A}_z &= 0 \\ \vec{n} \cdot \vec{J} &= 0 \end{aligned} \quad \text{Equations (V.5)}$$

Whith

$$\vec{n} = n_x \vec{i} + n_y \vec{j} + n_z \vec{k} \quad \text{Equations (V.6)}$$

And

$$n_x J_x + n_y J_y + n_z J_z = 0 \quad \text{Equations (V.7)}$$



**Figure V. 3 :** Boundaries of the domain of study of the dual-layer inductor

### 3. SIMULATION RESULTS AND DISCUSSION

#### 3.1. Current density distribution

The resolution of Maxwell's equations (equations V.1), using the finite element method [7], makes it possible to visualize in 3D the distribution of the density of the electric current (Figures V.4- V.5 and V.6) in the dual-layer inductor with different thicknesses and gaps.

For the smaller thickness of the conductor (60  $\mu\text{m}$ ), we observe a higher current density in the edges of the conductors facing the internal diameter, whatever the thickness of the gap. This phenomenon is generated by the inverse proximity effect and the important magnetic flux density at the dual layer inductor's center. The non-uniform current density induces non-homogeneous resistances in the conductors [8-11]. The current density in edges of conductors become less important when the conductor thickness becomes greater. This observation is confirmed by figures V.5 and V.6.

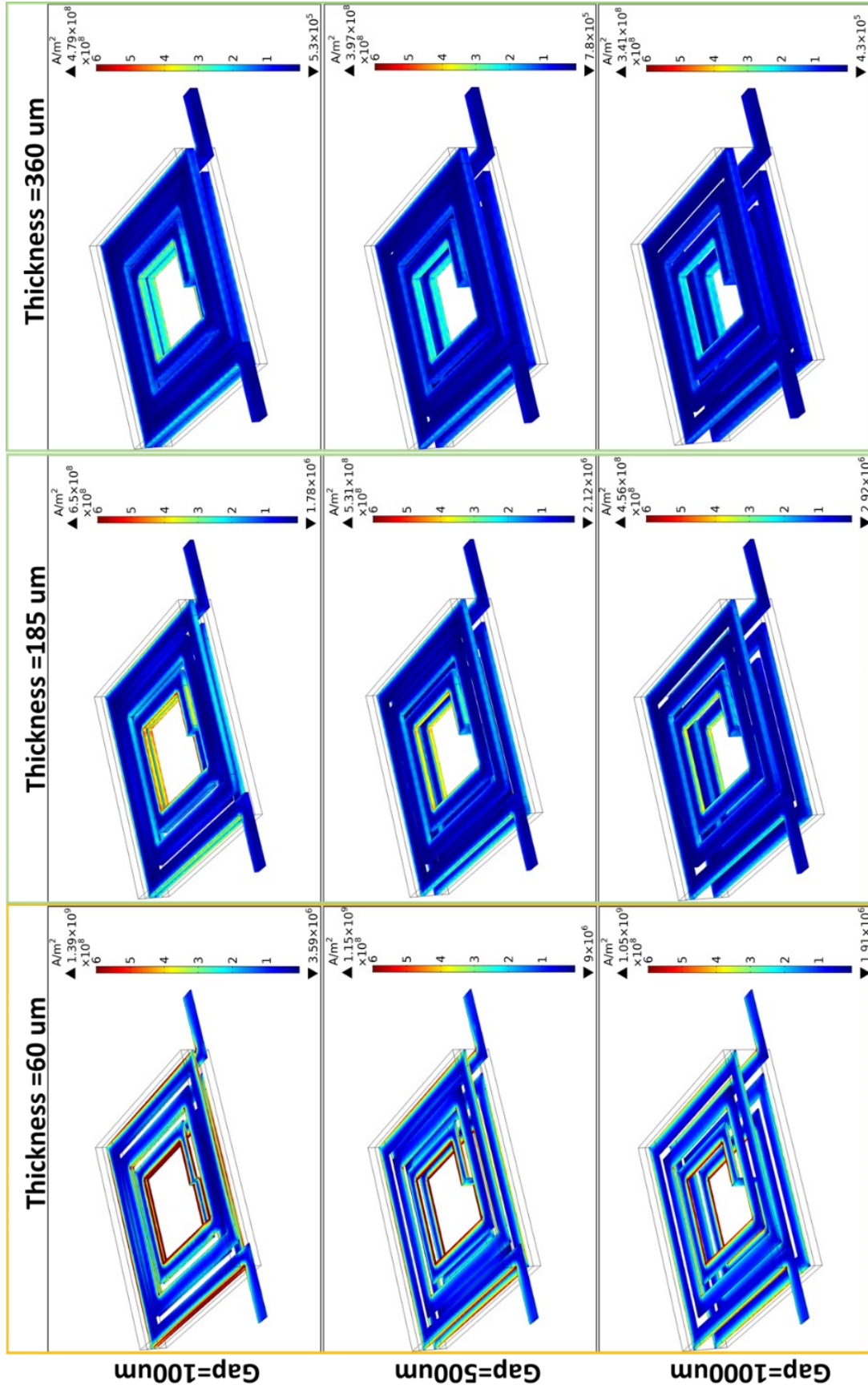
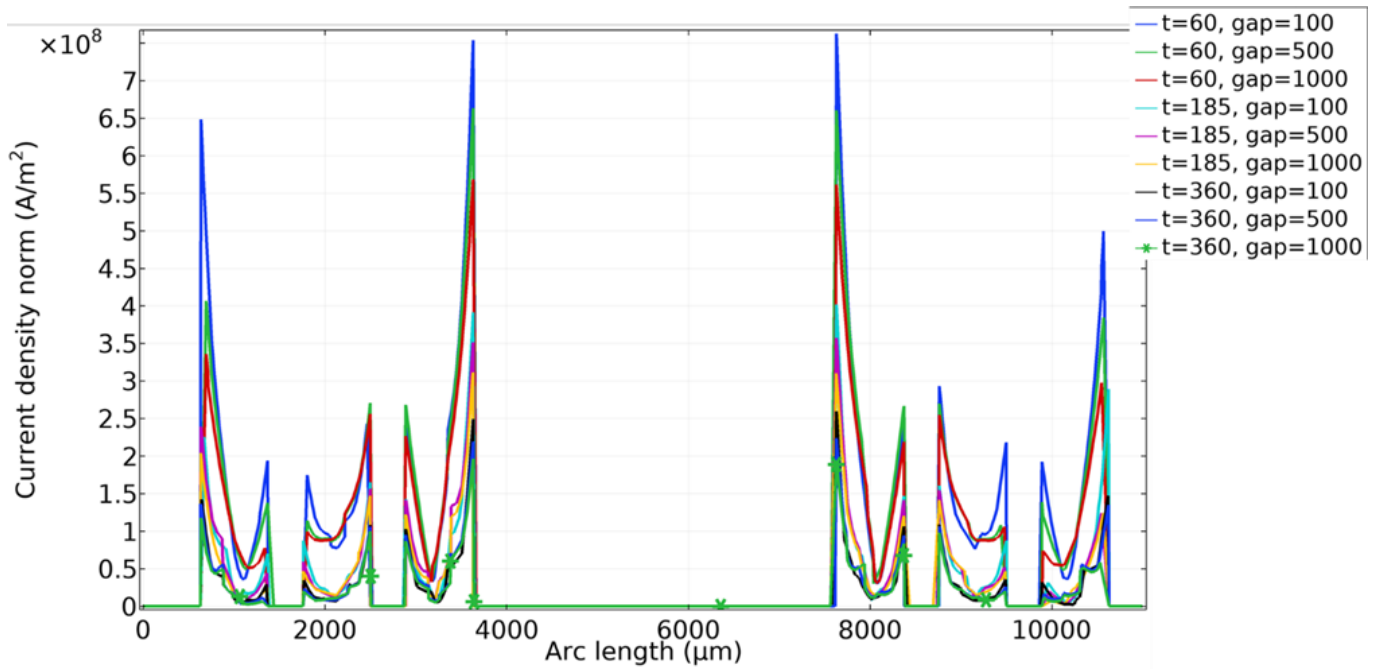


Figure V. 4 : 3D presentation of the current distribution in the winding of the dual-layer inductor with MPP magnetic core

To study the influence of the gap on the current density inside the conductor, we have plotted the curves of figure V.5. We notice That the proximity effect is more intense for the smallest gap, and becomes weaker as the gap widens. So, we conclude that the gap affects the current density inside the conductor and a very narrow gap is not recommended. Results of figure V.6 validate those of figure V.5.

If we compare figure V.5 and figure III.11 (Chapter III), we also, found that the insertion of the magnetic core has increased the current density., because of the increase of the magnetic flow.



**Figure V. 5:** Evolution of the current density according to the arc length crossing the top coil for each case.

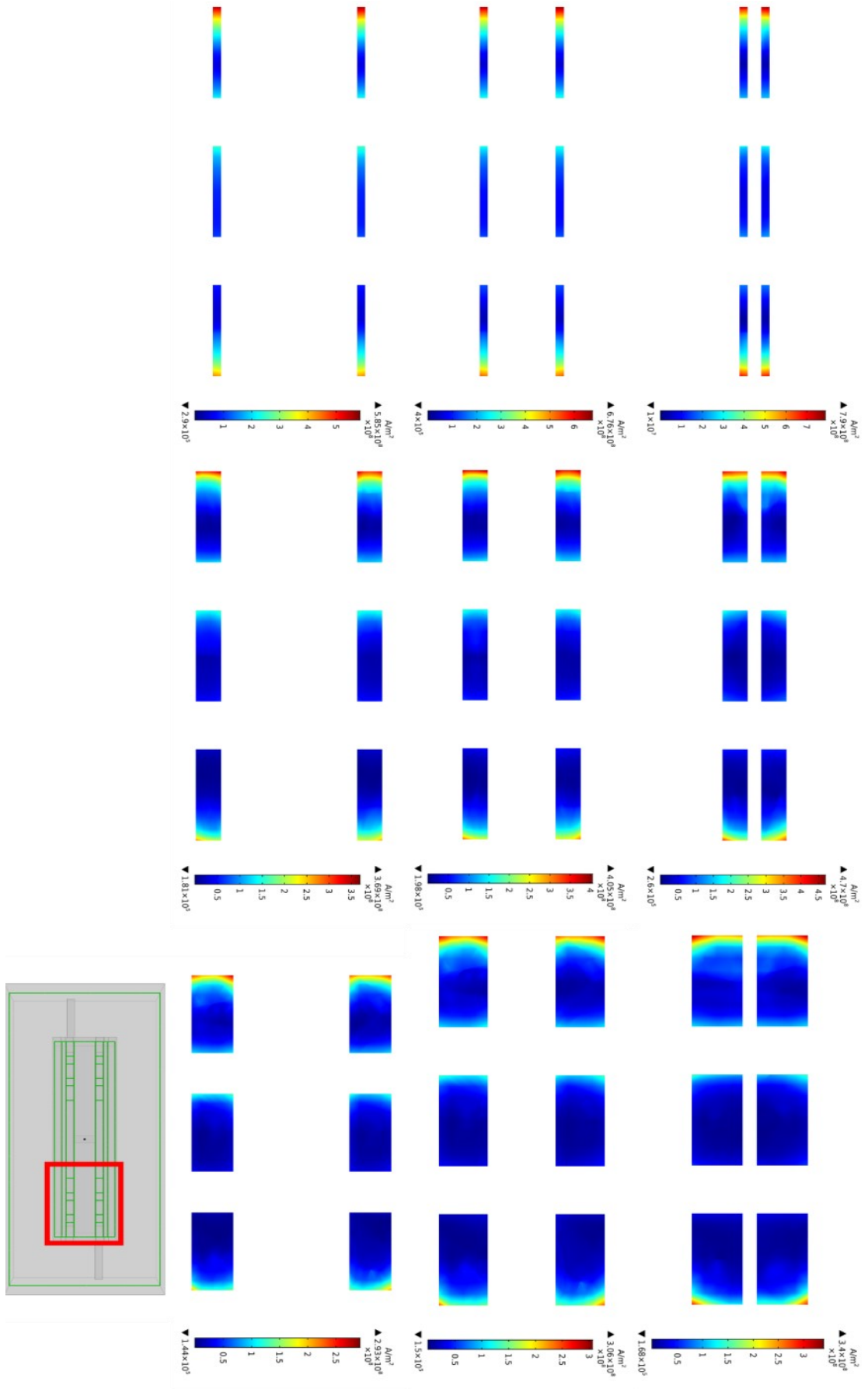


Figure V. 6: Cross section presenting the current distribution inside the inductor winding

### 3.2. Distribution of the magnetic field

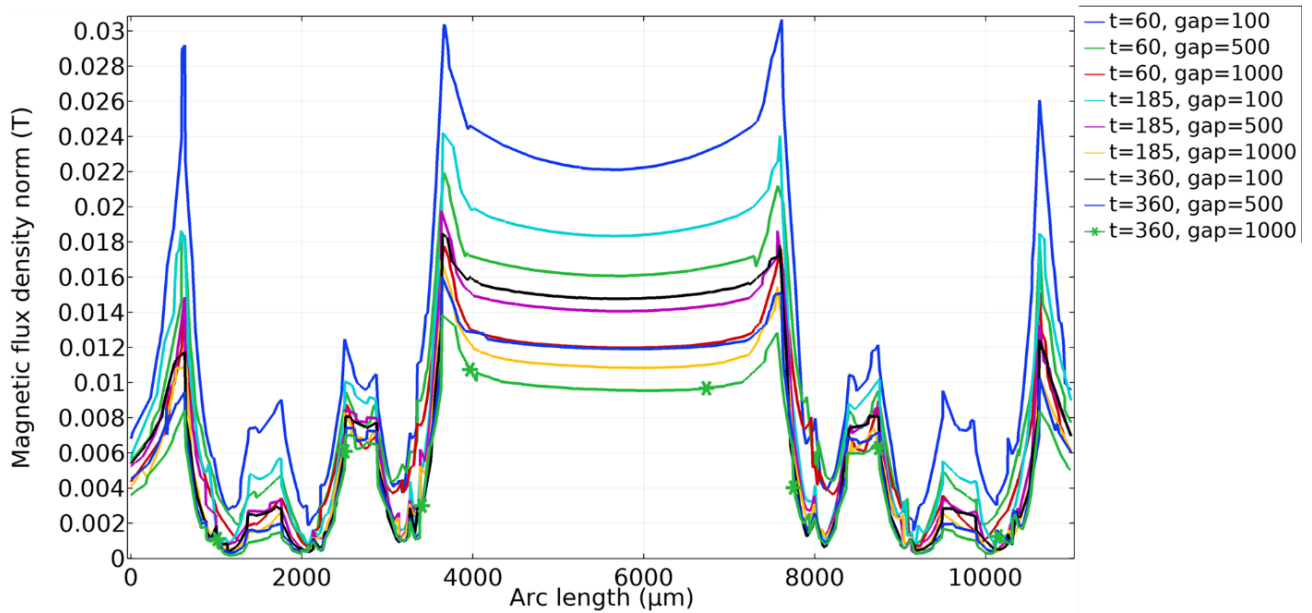
The distributions of the magnetic flux density and the magnetic field lines in the dual-layer inductor simulated by COMSOL Multiphysics are given by figures V.7, V.8 and V.9.

The magnetic flux density has a high value in the MPP magnetic core particularly, in the area covered by inductor winding, contrary to the centre (Figures V.8 and V.9).

A high magnetic flux density was recorded in figure V.7 for the inductors with the thin winding. It is also noticed, that the thin gap drives for a high flux magnetic compared to inductors with a large gap.

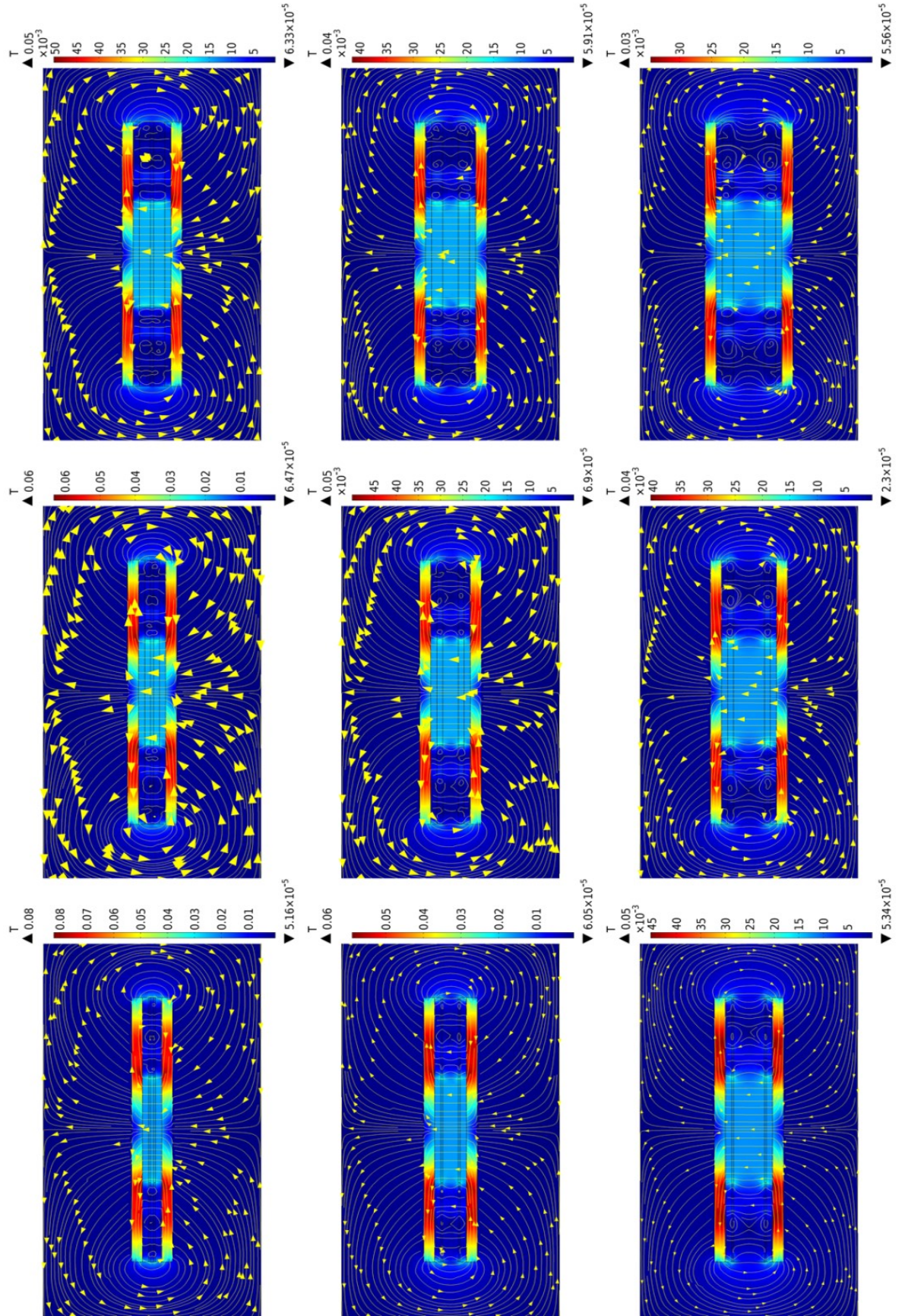
The maximum magnetic flux recorded for all cases didn't reach the saturation flux of the molypermalloy powder core which is 0.8 T.

In literature [12-17] the simulation of the single planar inductor shows that the magnetic flux is more intense at the coil centre. A different behaviour is shown in results of our dual-layer inductor. This behaviour is in favour of our inductor, because an intense flux at the centre of a miniaturized component leads to its heating and maybe, to a change in state of the materials that compose it. In this case, the electrical characteristics of materials change and disturb the operation of the inductor. Figure V.8 provides an explanation of this phenomenon.

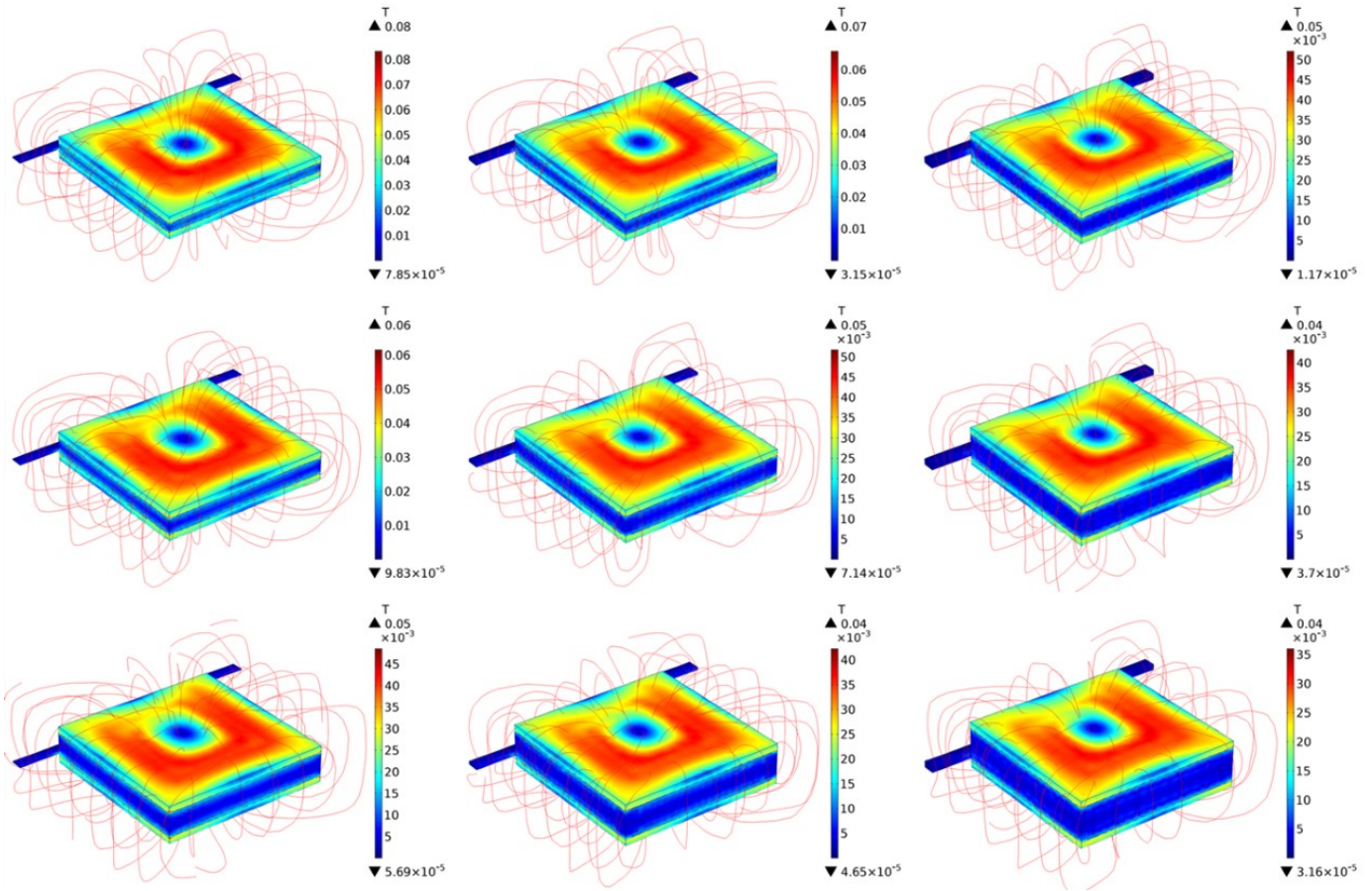


**Figure V. 7:** Magnetic flux distribution according to the arc length crossing the top coil for each case





**Figure V. 8 :** Cross section presents the magnetic flux and the magnetic field lines distribution in the inductor



**Figure V. 9:** 3D presentation of the magnetic flux and the magnetic field lines distribution in the inductor

#### 4. THERMAL SIMULATION OF THE DUAL-LAYER INDUCTOR

Currently, the development of electronic systems requires less voluminous passive components. But the miniaturization of these components promotes the increase in temperature due to the reduction of the volume, resulting in a permanent increase in the heat flow emitted by these systems. To solve this problem, the study of the thermal phenomenon during the design is strongly advised.

Our main objective in this part is to study the distribution of the temperature in the dual-layer inductor, as well as the heat transfer in its different stacked materials.

By using COMSOL Multiphysics simulation software, we have got the results presented in Figures V.11 and V.12. These results are obtained by solving the heat equation using the finite element method.

Figures V.11, and V.12 and table V.1 give a very clear idea about the temperature distribution in the dual-layer inductor.

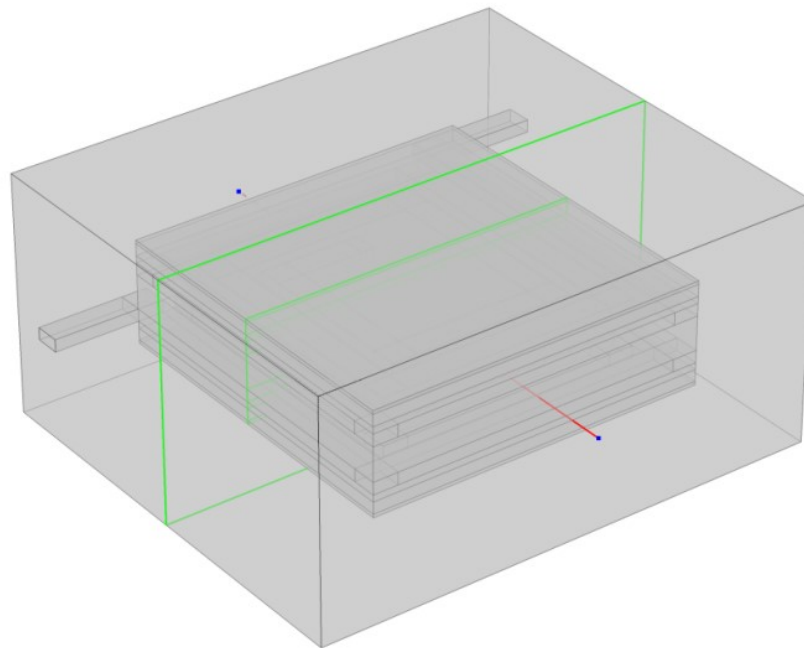


The inductor with thin winding shows a high temperature. It can be explained by the intense density of the magnetic flux and the high series resistance. We also find that the narrowest gap shows the highest temperature, because a narrow gap doesn't facilitate the evacuation of heat flux.

When the gap is associated with the thinnest conductor thickness ( $t=60\mu\text{m}$ ), it strongly influences the inductor's temperature; For example, a temperature difference of  $6.9^\circ\text{C}$  is recorded between the  $100\mu\text{m}$  gap and the  $500\mu\text{m}$  gap. On the other hand, the gap shows a weak influence on the temperature of the inductor when the conductor thickness increases, for example, the temperature difference recorded between the gaps of  $100\mu\text{m}$  and  $500\mu\text{m}$  is of the order of  $2.1^\circ\text{C}$  for the  $180\mu\text{m}$  thickness and of  $1^\circ\text{C}$  for the  $360\mu\text{m}$  thickness. These phenomena can be explained by the leakage currents which appear in large numbers when the conductive winding is thinner or the gap is narrower.

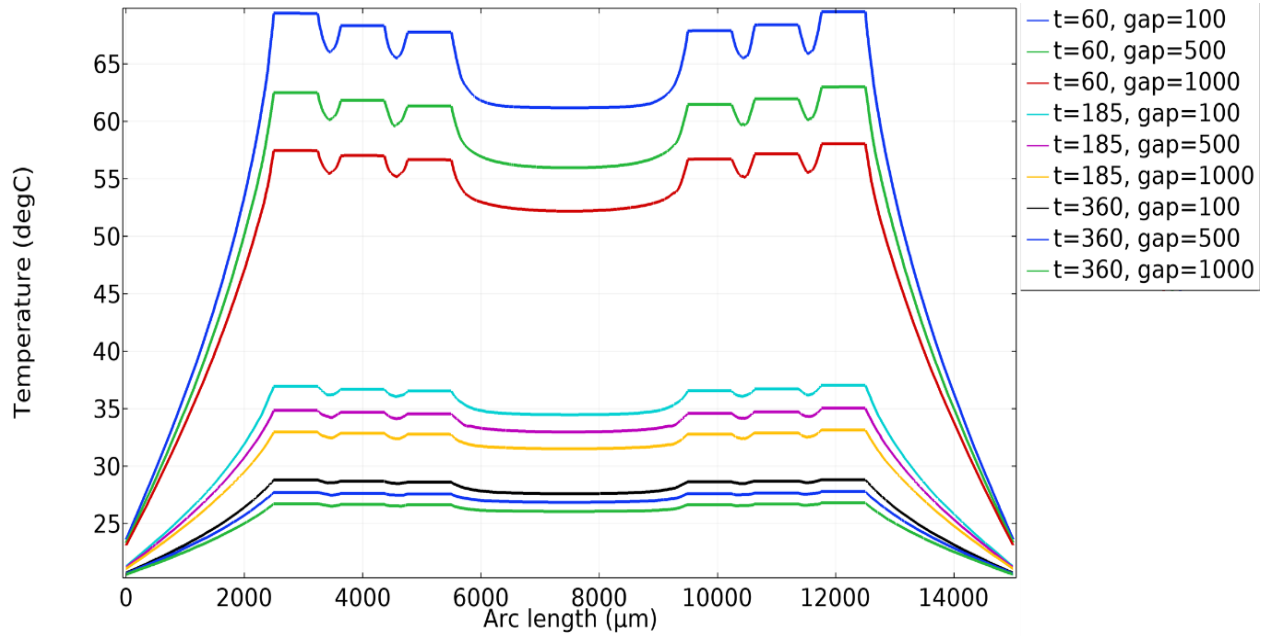
We came to the conclusion of an inversely proportional relationship between the gap and the inductor temperature.

Figure V.11 and V.12 are realized according to the vertical section of figure V.10

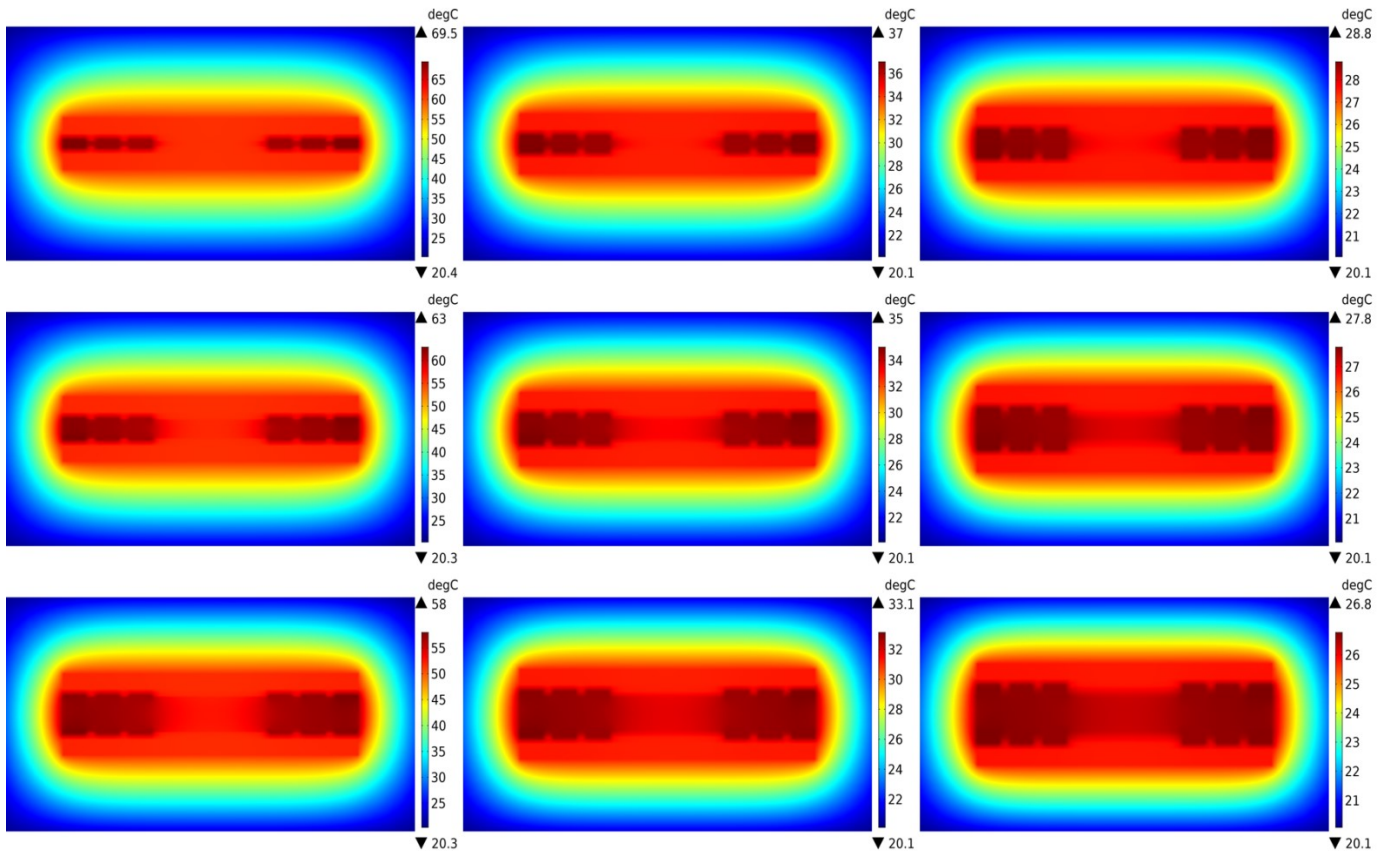


**Figure V. 10 :** Vertical arc for the temperature simulation

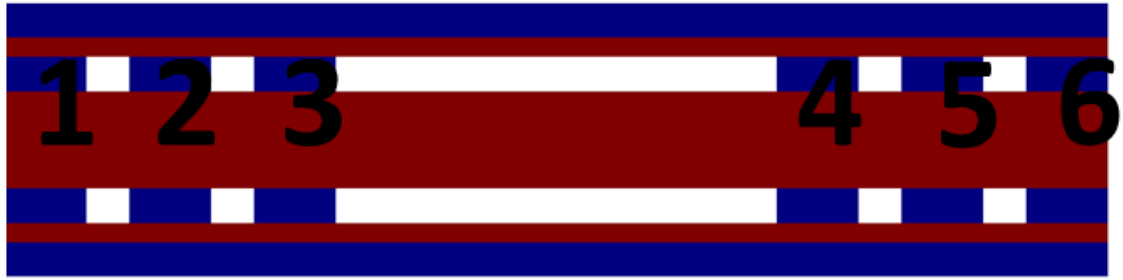




**Figure V. 11:** Heat flux distribution according to the arc length crossing the top coil for differents cases



**Figure V. 12:** Cross section presenting the heat flux in the dual-layer inductor.



**Figure V. 13:** Cross section of the dual-layer inductor

Table V.1 is realized according to the cross section of the dual-layer inductor shown in figure V.13.

segment	1	2	3	inner	4	5	6
60/100	69,4	68,3	67,8	61,1	68,9	68,4	69,6°
60/500	62,5	61,8	61,3	55,9	61,4	61,9	63
60/1000	57,4	57	56,6	52,1	56,7	57,1	58
185/100	36,9	36,6	36,5	34,4	36,5	36,7	37
185/500	34,8	34,6	34,5	32,9	34,6	34,7	35
185/1000	32,9	32,8	32,7	31,5	32,7	32,9	33,1
360/100	28,7	28,6	28,6	27,5	28,6	28,7	28,9
360/500	27,7	27,6	27,5	26,8	27,6	27,6	27,7
360/1000	26,7	26,6	26,5	26	26,6	26,6	26,7

**Table V. 1:** The temperature values measured for the different cases

The literature [12-13] indicates that the single-layer planar coils thermal simulation shows a significant heat flux at the inner winding, unlike the dual-layer inductor where the outer turns are more hotter than the inner turns and the temperature at the centre is the lowest (Table V.1). This phenomenon finds its explanation in figure V.8. This figure shows that in the dual-layer inductor the majority of the magnetic field lines cross its centre, while others loop the outer turns of the two stacked coils, contrary to the single-layer planar coil where all the magnetic field lines pass through the centre. This distribution of the magnetic field lines results in the cooling of the dual-layer inductor centre and slight heating of the outer turn.

Following the different comparative studies presented in chapters II, IV and V which directed us to the choice of the optimal conductor thickness and the optimal gap width, we came out with the following results:

To avoid accentuated skin and proximity effects, high leakage currents, high temperature and a low-quality factor, we opted for the thickness  $t = \delta = 180\mu m$  which gives the best results. the thicknesses  $t \prec \delta$  and  $t \succ \delta$  were rejected.

Our studies have also shown that a very small gap promotes the displacement of leakage currents outside the conductor, accentuates the proximity effect and shows a higher temperature than that of wider gaps. For these reasons, we have rejected the smallest gap ( $D_g=100\mu\text{m}$ ). The gap  $D_g=1000\mu\text{m}$  gives results as better as those of the gap  $D_p=500\mu\text{m}$ , except for the quality factor which is slightly lower, and a larger inductor volume. So, we opt for the gap  $D_g=500\mu\text{m}$ .

## 5. CONCLUSION

To consolidate our research for the choice of the optimal conductor thickness and the optimal gap, we have studied in this chapter V the electromagnetic and thermal behaviour of the dual layer inductor for different thicknesses and different gaps.

Using the COMSOL Multiphysics software, we have simulated several electromagnetic and thermal parameters, such as: the current density in the inductor winding, the magnetic flux and magnetic field lines distribution, also, the thermal behaviour of the inductor.

The numerical simulations have shown that the gap between the two stacked coils has a significant impact on the performance of the dual layer inductor. the small gaps cause a rise of magnetic flux density and temperature rise and favours a large circulation of leakage currents. All these adverse effects degrade the performances of the inductor.

A very thin winding also has a negative impact on the operation of the dual-layer inductor.

The simulation of the magnetic field lines for different gaps and thicknesses has shown a correct distribution and similar to that of classic inductors.

The simulation of the thermal effects has shown that the dual-layer inductor has the advantage of a lower temperature at its centre, unlike single layer inductors where the highest temperature is recorded at the centre.

These simulations were very beneficial to us in avoiding certain defects and designing a dual-layer inductor with very small dimensions, capable of operating correctly with better efficiency.

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# General Conclusion

## GENERAL CONCLUSION

The development of photovoltaic solar energy has taken a new dimension, on a global scale, following the awareness of the environmental challenge linked to global warming and the need to develop renewable energies which do not emit CO<sub>2</sub>. Therefore, it is important that research be initiated in the different fields of photovoltaic energy for profitability, reliability, and cost reduction.

A large number of researchers want to improve the yields of solar cells, which makes it possible to gain surface power and therefore reduce the cost of the Watt peak only. It should be noted that the development of photovoltaics is not based solely on the yields of solar cells but also on the improvement of equipment linked to PV panels.

The cost of photovoltaic installations is currently a major obstacle to their development. In the context of the integration of choppers, a significant reduction in volume necessarily leads to a reduction in cost. Therefore, it is important that a PV installation can produce the maximum possible energy at a lower cost. To this end, our objectives in this doctoral thesis aim to increase the profitability and reliability and, in particular, the cost of photovoltaic installations by reducing the size of static converters, which are numerous and occupy a large volume.

Our main objective is to design DC/DC miniaturized converters for photovoltaic energies, which can be inserted at the back of the PV module. These converters will be equipped with a correction block capable of maintaining the output voltage stable, regardless of the input voltage received from the PV panel.

Our starting point in this research work was the development of the specifications for a Boost DC/DC converter connecting the photovoltaic module to the inverter. After calculating the converter parameters responding to the specifications, we validated the proper functioning of the chosen converter using the PSIM simulation software.

It is obvious that any drop in the input voltage coming from the PV panel affects the output voltage, and it is known that the voltage delivered by the PV module cannot be stable due to various external parameters, such as the shading effect on the surface of panels or the effect of different orientation angles, the effect of dust etc. To correct this defect and maintain the output voltage of the Boost converter stable, we have designed an MPPT system that controls the converter by a square signal with a variable duty cycle  $D$  allowing us to stabilize

output voltage at the desired voltage. Once we had developed this system, which gives the converter the possibility of self-correcting, we went to the converter miniaturization stage.

The miniaturization of a Boost converter necessarily involves the miniaturization of its passive components, which occupy 80% of its volume. In this work, our concern is the coil which is the centrepiece of the converter.

In the literature, planar spiral inductors with a volume of  $\text{mm}^3$  and  $\mu\text{m}^3$  are known as an alternative to conventional coils with a very large volume. But these inductors are not yet well mastered and require a lot of adjustments.

Following a bibliographical study, our choice fell on a coil of the planar spiral type with two stages to benefit from the mutual inductance and increase the value of its overall inductance.

To minimize energy losses and ensure the proper functioning of our dual-layer inductor, a comparative study was carried out to choose the optimal conductor thickness and the optimal gap between the two stacked windings because these two parameters are very disturbing elements. The conductor thickness is a major factor in losses by Joule effects and losses by capacitive effect, and a poorly dimensioned gap can generate intense leakage currents between the stacked windings.

The design of the electrical circuit of the dual-layer inductor allowed us to simulate the output voltage of the converters for different binomials (thickness, gap). The simulations carried out by the PSIM software showed the binomial, which gave the best result and allowed us to test our designed corrector block.

The obtained results showed the very good operation of the corrector block, which adjusted all the voltages to 220 V with an error (the error required by the specifications).

We can say that this corrector block associated with the Boost converter will be very useful for the gain of photovoltaic energy.

A good geometrical dimensioning is not sufficient to affirm that the inductor, once carried out, works correctly because other parameters can intervene during its operation, such as rather high-temperature heating of the inductor and the converter, or a saturation of the magnetic core, etc. For this reason, all electromagnetic and thermal parameters have been studied using the COMSOL Multiphysics simulation software.

Results of simulations show that a very thin winding and a very small gap are

not recommended, and the thermal simulations results indicated that the dual-layer inductor has the lowest temperature at its centre, unlike the single-layer inductor, where the highest temperature is recorded at its centre.

This research was very beneficial for us in avoiding some defects which harm the miniaturization of planar inductors and to design a dual-layer inductor with very small dimensions, capable of operating correctly with better efficiency. This dual-layer inductor can also ensure the operation of a converter delivering an 80 W power.

We can say that the obtained results are very satisfactory, and part of them have been published in an international scientific journal, with an article entitled "Miniaturization and Optimization of a DC-DC Boost Converter for Photovoltaic Application by Designing an Integrated Dual-Layer Inductor Model."

It should also be noted that the design of this converter model was proposed as a Start-Up project entitled "Easy Energy" at the second edition of TECH BOOST Bootcamp Algeria, organized by Brenco in partnership with THE OFFICE and ANIMA Investment Network as part of THE NEXT SOCIETY program funded by the European Union. Our project was ranked as the third-best project nationwide.

Among our perspectives for the near future: the realization of a Boost converter with the corrector block, as well as the dual-layer inductor.