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Study and Simulation of a Nanoscale Structure of a Multi-gate MOS Transistor

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Declaration

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Publications

- **N. Boukortt**, B. Hadri, S. Patanè, A. Caddemi, and G. Crupi, "Investigation on TG n-FinFET parameters by varying channel doping concentration and gate length" Silicon - Springer (2016).
- **N. Boukortt**, B. Hadri, A. Caddemi, G. Crupi, and S. Patanè, "The temperature dependence of electrical parameters of TG SOI n-FinFET" Trans. Electr. Electron. Mater. (2016).
- **N. Boukortt**, B. Hadri, S. Patanè, A. Caddemi, and G. Crupi, "Electrical Characteristics of 8-nm SOI n-FinFETs" Silicon - Springer (2016).
- **N. Boukortt**, B. Hadri, and S. Patanè, "Effects of high-k dielectric materials on electrical characteristics of DG n-FinFETs" IJCA (2016).
- **N. Boukortt**, B. Hadri, and A. Caddemi, "Simulation of a Nanoscale SOI TG n-FinFET" IJCA (2016).
- **N. Boukortt**, A. Caddemi, E. Cardillo, G. Crupi, B. Hadri, and S. Patanè, "Inverse Modeling of an AlGaAs/GaAs HEMT from DC and Microwave Measurements" 12th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services – TELSIKS, IEEE Proceeding Conference. (2015).
- **N. Boukortt**, B. Hadri, L. Torrisi, S. Patanè, A. Caddemi, and G. Crupi "Influence of gate dielectric materials on electrical characteristics of 3D DG n-FinFETs with different channel materials" Nanotech France 2015 International Conference Proceeding (2015).
- **N. Boukortt**, B. Hadri, A. Caddemi, G. Crupi, and S. Patanè, "3-D Simulation of Nanoscale SOI n-FinFET at a Gate Length of 8 nm Using ATLAS SILVACO" Trans. Electr. Electron. Mater. 16, 2-7 (2015).

Further publications arising from this thesis are in preparation.

Abstract

To enable the advancement of Si based technology, necessary to increase computing power and the manufacture of more compact circuits, significant changes to the current MOS multi-gate transistor device are a necessity. Novel transistor architectures and materials are currently being researched vigorously. This thesis, on the electrical characterisation of multi-gate transistors displays detailed insight into the carrier transport and resulting performance limiting mechanisms. The results are composed of many parts. The impact of variations of the gate length, gate dielectric material, fin parameter, gate work function, doping concentration, and temperature on device characteristics are studied using ATLAS Silvaco device simulator. Simulation results for various gate lengths are reported and analyzed. As the quantum effects are pronounced in nanoscale devices, we have included these effects in our study and simulation. We have then compared the achieved results to classical simulations to assess their performance limits. Finally, a comparison of our results with recently published data is presented to confirm our study.

Keywords: Nanotechnology, Scaling, FinFET, Leakage current, Gate length, Silvaco Software.

CHAPTER I: Introduction

1.1 Work Overviews

The aim of this work was the optimization of MOS multi-gate transistor device performance using Semiconductor TCAD tools. Semiconductor TCAD (Semiconductor Technology Computer Aided Design) tools are computer programs which allow for the creation, fabrication, and simulation of semiconductor devices. These tools were used to optimize semiconductor devices for various applications.

During the course of this work, these programs were used to create simulations of the devices being worked on. These simulations provided the opportunity to study the effect of different device parameters on the overall device performance. Throughout the years, the devices were simulated and gradually the performance of each one was improved, until an optimal device configuration was created for the particular applications.

1.2 Objectives

The overall objective of this project was the optimization of the various semiconductor devices. In order to achieve this goal, several intermediate objectives were needed.

- Understand FET devices and the applications for which it is used
- Learn and understand the use of Silvaco's TCAD software
- Create an initial device design using reference material from Silvaco's web-site
- Generate benchmarks for initial device design
- Choose an application for which the device is to be optimized
- Vary device parameters and study resulting effects upon performance
- Determine optimal values for FinFET device parameter
- Combine the optimal parameters into a final, fully optimized device

The accomplishment of each of these intermediate objectives was critical to the success of the work as a whole. All these objectives can be grouped under three main categories and are expanded upon in the following section.

1.3 Project Definition

1.3.1 Understand the Devices

First and foremost a basic understanding of the fabrication, operation, advantages, and applications of FET (Field Effect Transistor) device was needed before any simulations or optimizations could commence. This understanding of the devices was gained through extensive research conducted on each device. Various sources were consulted and the resultant understanding of the devices was key in the creation of optimized device configurations.

Two devices were selected for optimization during the course of this work. These devices are the SOI FinFET (Fin-Shaped Field Effect Transistor) device and the triple gate

FinFET device. An in-depth report on the research conducted can be found under each individual device section. For the purposes of the introduction, a general device overview is given.

FinFET technology is a new industry standard. This technology has been around for recent years, and the fabrication methods are continually improving, yet they are well established [1].

The cost and size are main advantages of FinFET devices. Since the technology is well established, fabrication methods have become relatively inexpensive. Also, the device itself is physically smaller than other technologies, allowing for the placement of more devices on a silicon wafer during fabrication. FinFET devices are mainly used in the creation of CMOS logic chips, which are at the heart of every computer [1]. An enhancement-type NMOS transistor was used during the course of this work which has high electron mobility and interfaces easily with low voltage positive logic compared to PMOS. Figure 1.1 shows the basic structure of this style FinFET device.

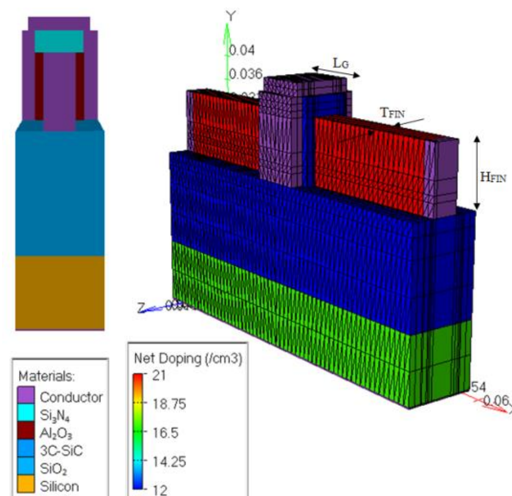

Figure 1.1 Physical structure of an enhancement-type n-FinFET transistor [1].

SOI (Silicon-On-Insulator) devices are a relatively new technology. Although the technology has been available since the 1960's, SOI devices are only recently becoming commercially viable, due to the expense associated in producing the devices. SOI devices are an advancement of standard FinFET technology. The main difference between SOI and bulk technology is the inclusion of an insulating layer. SOI devices are created from a thin layer of silicon placed on top of a layer of insulating material [2]. This structure can be seen in Figure 1.1. Most often this material is silicon oxide, however other insulating materials are being tested, such as diamond, sapphire, and ruby. For this work, a buried oxide layer (BOX) of silicon dioxide was used for the creation and simulation of the SOI FinFET device [2].

The second technology for which optimization was pursued is the TG n-FinFET (Triple Gate n-FinFET) device. This device takes advantage of the buried oxide layer of a SOI device by adding a third gate above the device's channel. This allows for greater control of the device switching, and opens the doors for great advances in device design. The FinFET

technology is by far the newest and most advanced semiconductor technology simulated during the course of this work, further explanation of this device and the others simulated during the work, can be found under the individual device sections.

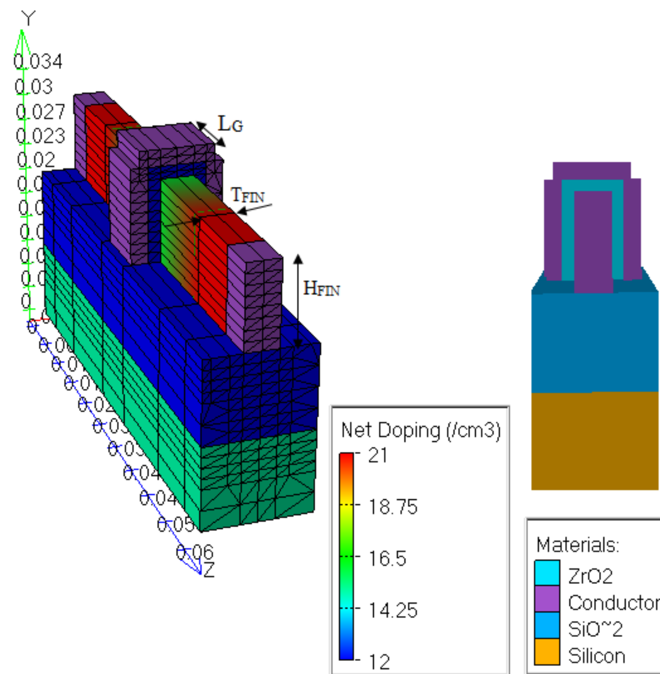

Figure 1.2. Physical structure of an enhancement-type TG n-FinFET transistor [3].

1.3.2 Learn the Usage of the Software Package

Once a basic understanding of each device was acquired, and in some cases while research on the device was proceeding, the operation of the software package needed to be learned. The software package used for this project is Virtual Wafer Fab (VWF) package built by Silvaco International. VWF is a suite of software programs used to create a multi-functional environment for the simulation of semiconductor technology. Several different programs were learned and then used throughout the years, allowing for simulation of these devices on many different levels. After trying different programs in the suite, simulation efforts were focused on using ATHENA, ATLAS, DevEdit, and DeckBuild [4].

ATHENA is a framework program that integrates several smaller programs into a more complete process simulation tool. It is a modular program that combines one and two-dimensional simulations into a more complete package allowing for the simulation of a wide range of semiconductor fabrication processes. This program's focus is upon the simulation of fabrication processes. In ATHENA, devices are created through simulation of the fabrication process [4].

ATLAS is a device simulation tool. The framework of ATLAS combines several one, two, and three-dimensional simulation tools into one comprehensive device simulation package. This allows for the simulation of a wide variety of modern semiconductor

technologies. Devices can be created in ATLAS through layout based simulation syntax; however the main focus of this program is simulation of the device once fabrication is complete [4].

DevEdit is a program that allows for structure editing, structure specification, and simulation grid generation. All of Silvaco's programs use a mesh or grid to determine the level of detail that the simulation will generate in a specific area of the device, allowing users to cut down on simulation time by removing detail from areas with uniform or no reaction to performance simulations. The creation of these meshes is the main function of DevEdit, however it is also be used for the editing and specification of two and three-dimensional devices created with the VWF tools [4].

DeckBuild is the front-end GUI (Graphical User Interface) for Silvaco's Virtual Wafer Fab programs. This program is the framework which ties together the wide range of process and device simulation tools available, and allows them to work together seamlessly and efficiently [4]. DeckBuild uses pull-down menus to generate syntax for the various programs, and provides basic simulation controls such as stop, pause, and restart. The use of ATHENA, ATLAS, and DevEdit are expanded upon in later sections of this thesis, DeckBuild was used for front-end simulation control in each case. In order to learn the use of these programs, many sources were consulted [4].

Various device examples are available through the Silvaco's homepage. These examples and research material available through the company's web-site and user manuals have been used as starting point to gain the basic knowledge of each program's operation. Once this operational level of understanding was acquired, research into the effects of device parameters upon performance could begin.

1.3.3 Simulate and Optimize Devices

Once an understanding of the device and the software was obtained, the simulation and optimization of the devices could begin. The first step in optimization is the selection of an initial device configuration. Using reference material and example programs available through Silvaco's homepage, initial device designs were created, taking into account the computing time. These initial configurations were designed to be simple, yet straightforward examples each device's capabilities.

Once initial devices were selected, a goal for optimization was needed. It was decided that the devices would be optimized for low power, high-speed applications. In order to determine the optimal configuration, the I_D vs. V_{GS} curves were examined. A lowered threshold voltage and an increased transconductance became the optimization goals of the work. Improving these two parameters would produce a lowered operating voltage, and increased switching speed. Optimization for reducing the subthreshold swing, DIBL, and leakage current were three other objectives considered for the work. However, after further research both these goals were determined to be beyond the scope of this work, and were ultimately removed from the list of design goals.

Optimization of these devices using the TCAD tools requires many hours of lab simulation time. Several aspects of each device were selected for optimization. First each parameter was tested individually for its effect on device performance as a whole. Once several plots were obtained that indicated the particular parameter's effect on device performance, improved values could then be selected for the device. Several simulations needed to be run to find improved values for each device parameter, until an optimal value was reached. After reaching the optimal value of each of the device parameters which should recombine them together into a single device, the simulation could begin to optimize based upon their combined effects and to ultimately produce an optimal device configuration.

1.4 Thesis Structure Overview

The remainder of this thesis focuses on each aspect of this research work in far more detail. Explanations the reasons for the choosing of each device structure used for simulation, the design methods used, detailed information about the function of each device, and step by step explanations of the steps taken during optimization. The MOS transistor is the first device discussed in this thesis due to the relative simplicity of the device. Once a basic understanding of the FET and the optimization approach for this device is grasped, the SOI devices become easier to understand. The SOI concepts are used as a foundation for understanding a new generation of FinFET devices.

Chapter II: FET Device Physics

The main components of an integrated circuit (IC) are Metal-oxide-semiconductor (MOS) transistors. MOS technology is used in microprocessors, microcontrollers, static RAM, SRAM cell, and other digital logic circuits. Also, it is used in a wide variety of analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of applications [5]. Two important characteristics of the Complementary MOS (CMOS) technology are high noise immunity and low static power consumption. Significant power is only drawn when the transistors are switching between on and off states. Consequently, MOS circuitry dissipates less power and is denser than other implementations having the same functionality. As this advantage has grown and become more important, the vast majority of modern integrated circuit manufacturing is on CMOS processes. Currently, the appearance of smart devices such as smartphone, tablet, and laptop changes semiconductor market trends. The origin of smart devices was IBM Simon which was released in 1993 as a world first smart device as a convergence between mobile phone and PC [2, 5]. It included a schedule manager, address book, world clock, fax, games, and calculator etc. With evolutions, smart devices have been continuing like personal digital assistant, iPhone and Galaxy Tab etc. Especially after iPhone and Android smartphone has been released in the market, numerous smart applications which use simple user interface, global positioning system (GPS), motion sensors and Wi-Fi etc., play a role as a bridge between human and smart devices.

1. The metal-oxide-semiconductor-field-effect-transistor

A standard semiconductor MOSFET consists of a MOS capacitor with a highly doped source and drain region either side (Figure 2.1), each with a respective metal contact. These relatively simple devices can be p-channel (n-doped body with highly p-doped source and drain) or n-channel (p-doped body with highly n-doped source and drain). Figure 2.1 is a schematic of an n-channel MOSFET including the electrical connections. Note the source and p-type substrate are grounded. When $V_{gs} < V_{th}$, the p-type substrate is either in accumulation or depletion and no current can flow between the source and drain even when in the presence of the bias V_{ds}. The MOSFET acts like two *p-n junction diodes* connected back to back (two p-n junction diodes). When $V_{gs}>V_{th}$, the semiconductor surface is inverted to n-type, forming a conducting channel between the n+ source and drain. When V_{ds} is applied an electron current will flow from the source to the drain [6]. Increasing the gate bias increases the concentration of electrons at the semiconductor surface, and allows more current to flow [7].

The gate can therefore be used to modulate the current flow between source and drain, giving rise to the switching operation in integrated circuits.

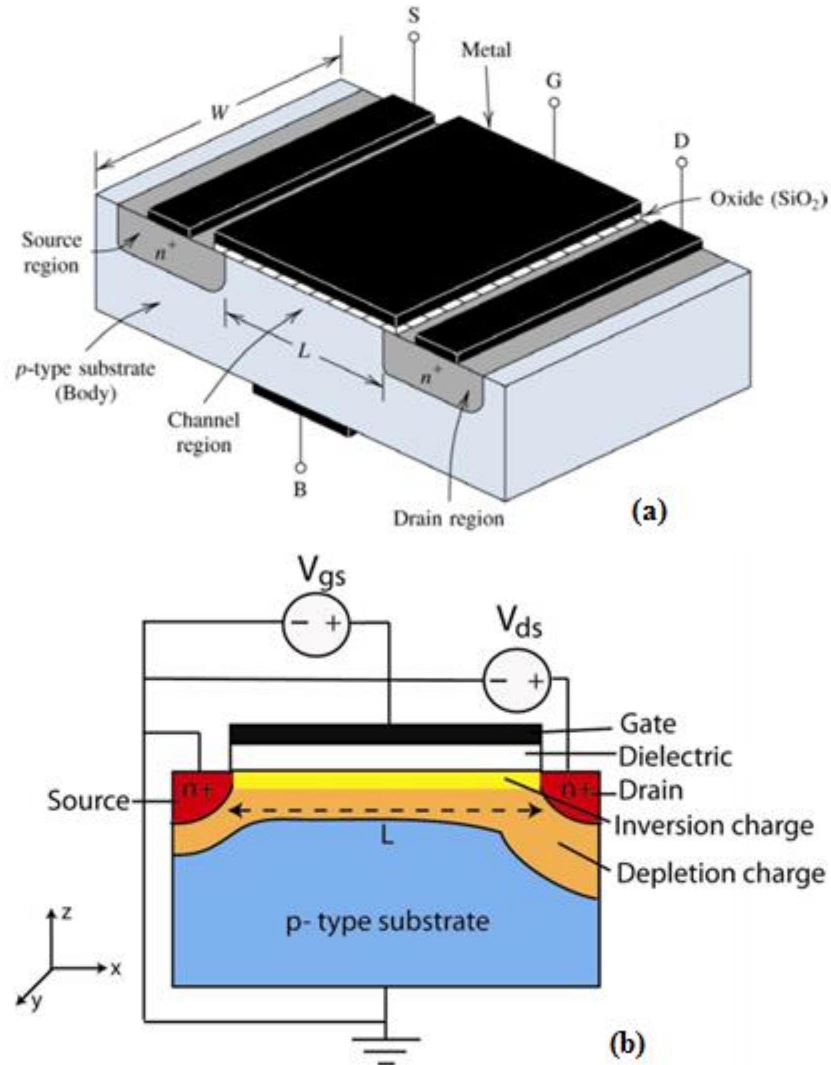

Figure 2.1 Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section [8].

1.1. The MOS capacitor

A MOS capacitor consists of a conducting metal layer (metal gate) on top of a dielectric grown or deposited on a semiconductor substrate, the bulk of which can be doped n-type (p-MOS capacitor) or p-type (n-MOS capacitor). The operation of an n-MOS capacitor under gate bias, V_{gs} is now considered. All potentials are with respect to the substrate/bulk which is grounded. At zero applied bias, the bending of the energy bands is ideally determined by the difference in the work functions of the metal and the semiconductor

(Band bending means a change in electric potential and therefore the existence of an electric field.) Oxide and interface trapped charges can also contribute to an appreciable amount of band bending [9, 10].

This band bending changes with the applied bias and the bands become flat when we apply the so-called flat-band voltage given by [11]:

$$V_{FB} = (\phi_m - \phi_s)/q = (\phi_m - X_s - E_c + E_F)/q \tag{2.1}$$

where ϕ_m and ϕ_s are the work functions of the metal and the semiconductor, respectively, X_s is the electron affinity for the semiconductor, E_c is the energy of the conduction band edge, and E_F is the Fermi level at zero applied voltage. The different energies involved are indicated in Figure 2.2, where it presents typical band diagrams of a MOS capacitor at zero bias, and with the voltage $V = V_{FB}$ applied to the metal contact relative to the semiconductor–oxide interface.

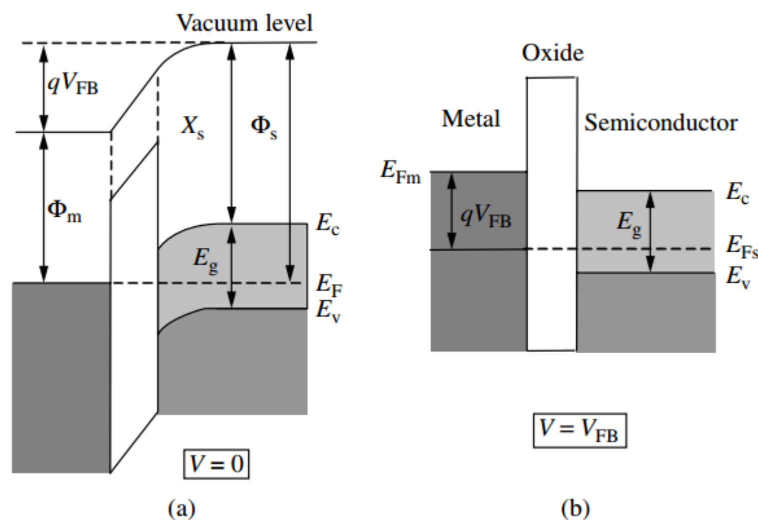

Figure 2.2 Band diagrams of MOS capacitor (a) at zero bias and (b) with an applied voltage equal to the flat-band voltage. The flat-band voltage is negative in this example [11].

In stationary conditions, no net current flows in the direction perpendicular to the interface, owing to the very high resistance of the dielectric layer. Hence, the Fermi level remains constant inside the semiconductor, irrespective of the biasing conditions [8]. Very little band bending occurs in the metal due to the abundance of free carriers. An n-MOS capacitor will enter the accumulation regime of operation when the voltage applied between the metal and the semiconductor is more negative than the flat-band voltage ($V_{fb} <0$). The negative bias raises the metal Fermi level (i.e. the potential energy of electrons) with respect

to the semiconductor Fermi level and creates an electric field from the substrate, through the oxide (just like an ordinary parallel plate capacitor) into the gate. Electrons in the gate are displaced towards the semiconductor and holes in the semiconductor displaced towards the gate. Figure 2.3a) shows the energy bands in accumulation. The field in the semiconductor causes the bands to bend upward. The Fermi level at the surface is now much closer to the valence band than the Fermi level in the bulk, corresponding to a much higher holes concentration at the surface than the equilibrium ones in the bulk. When $V_{gs} > V_{FB}$, the capacitor will enter the depletion regime of operation. The positive bias lowers the metal Fermi level with respect to the semiconductor Fermi level. The electric field is now in the direction from the gate to the substrate. Holes in the semiconductor move away (depleted) from the interface, leaving a net negative charge from the acceptor ions. This is known as depletion charge. The bands in the semiconductor bend downwards. The valence band at the surface is now farther away from the Fermi level than the valance band in the bulk expressing the lower holes concentration at the surface than the equilibrium ones in the bulk. As V_{gs} increases, holes continue to be depleted from the interface leaving behind more acceptor ions resulting in more depletion charge and a wider depletion region. This continues until it becomes energetically favorable for electrons to populate the conduction band at the surface. The process of electrons populating the conduction band at the surface in a p-type semiconductor is known as surface inversion and the surface behaves like an n-type material. The resulting sheet of electrons at the surface is referred to as the inversion layer. At this point all holes are depleted from the surface and the depletion charge ceases to increase. Figure 2.2b) shows the energy band diagram when the MOS capacitor is in the inversion regime [8-10].

On the energy band diagram, the bands bend downward so much that at the surface, which the conduction band approaches the Fermi level expressing the much higher electron concentration. In the figure, the Fermi level at the surface is as far above the intrinsic level, E_i, as the Fermi level is below the intrinsic level in the bulk semiconductor. Thus the electron concentration at the surface is the same as the holes concentration in the semiconductor. This condition is known as the threshold inversion point and the corresponding gate voltage known as the threshold voltage, V_{th}. The additional field lines from the gate now terminate on the inversion charge rather than the depletion charge, thereby screening the semiconductor from any further band bending. When $V_{gs}>V_{th}$, we enter into strong inversion where more inversion charge will be generated whilst the band bending remains essentially constant [8].

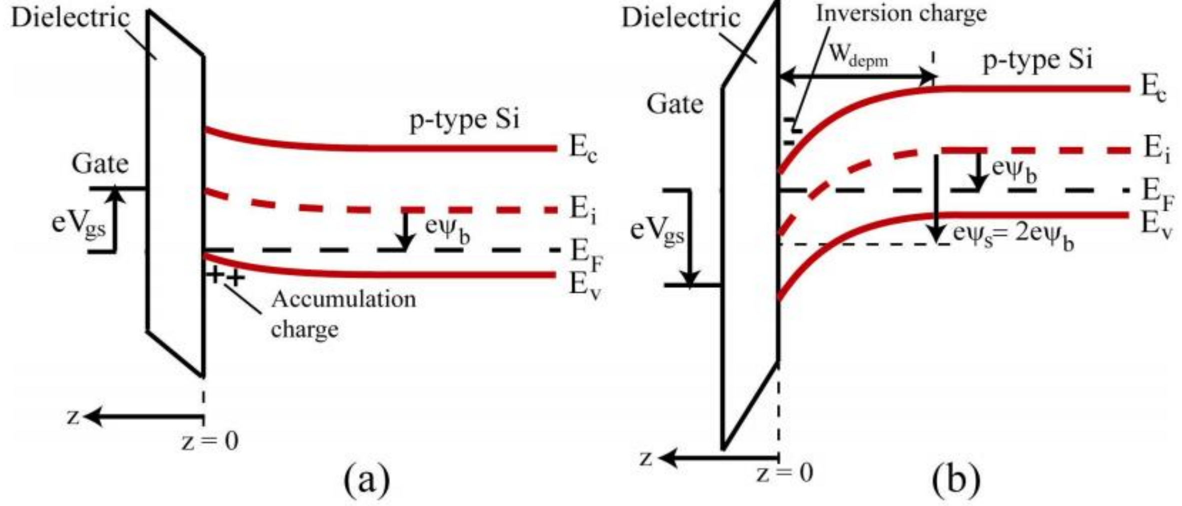

Figure 2.3 a) n-MOS capacitor in accumulation and b) inversion [8].

The gate voltage at inversion is related to the voltage across the oxide (V_{ox}), the semiconductor ψ_s, and flat-band voltage (V_{FB}) which is an important parameter when analysing capacitance profiles as it marks the boundary between accumulation and depletion [8].

$$V_{gs} = V_{FB} + V_{ox} + \psi_s = V_{FB} + \frac{Q_s}{C_{ox}} + \psi_s \qquad (2.2)$$

where C_{ox} is the areal oxide capacitance and Q_s is the areal total surface charge at the semiconductor-oxide interface, composed of the areal inversion and depletion charges, Q_{inv} and Q_{dep} respectively. It is common to express Q_{inv} and Q_{dep}, as inversion charge density N_{inv} and depletion charge density N_{dep} (normalised with respect to electron charge). ψ_s is the surface potential, is defined as the difference between the intrinsic Fermi-level (in V) at the surface and its bulk level. Note that the perturbations of the conduction band, valence band and intrinsic Fermi-level band are equal. The band perturbation potential as a function of distance perpendicular to the interface, $\psi(z)$ is a parabolic function. At the edge of the depletion region, $\psi(z = W_{dep}) = 0$. At the surface ($z = 0$) the band perturbation potential is equal to the surface potential $\psi\ (z = 0) = \psi_s$. W_{dep} is the width of the depletion region. Integrating Poisson's equation from the bulk to the interface gives an expression for $d\psi(z)/dz$. Depending on the regime of device operation, certain terms will dominate allowing the expression to be simplified. From which [8];

$$W_{dep} = \sqrt{\frac{2\ \varepsilon_{Si}\ \varepsilon_0\ \psi_s}{e\ N_a}} \qquad (2.3)$$

where ε_{Si} is the semiconductor relative permittivity, e is the electron charge, and N_a is the ionised acceptor concentration, which is normally approximately equal to the substrate doping concentration. The depletion charge per unit area is approximately:

$$Q_{dep} = eN_aW_{dep} \tag{2.4}$$

The surface potential at the onset of strong inversion [11]:

$$\psi_s = 2\psi_b = 2\frac{KT}{e}\ln\left(\frac{N_a}{n_i}\right) \tag{2.5}$$

where the bulk potential $\psi_b = \frac{E_F - E_i}{e}$ as shown in Figure 2.2. n_i is the intrinsic carrier concentration, k the Boltzmann constant, T the temperature .

At the inversion condition, the *depletion width reaches its maximum width W_{depm}*; obtained by substituting eqn. (2.5) into eqn. (2.3) [11].

$$W_{depm} = \sqrt{\frac{4\ \varepsilon_{Si}\,\varepsilon_0\,KT\ln(N_a/n_i)}{e^2\,N_a}} \tag{2.6}$$

1.2. Threshold voltage

Threshold voltage of the device is an important parameter which decides the device performance. The value of gate to source voltage (V_{gs}) for which sufficient amount of mobile electrons accumulates in the channel region so that a conducting channel is formed is called the threshold voltage. Combining the equations above, V_{th} can be expressed in the following form [10];

$$V_{th} = V_{FB} + 2\psi_b + \frac{\sqrt{2\,\varepsilon_{Si}\,\varepsilon_0\,e\,N_a\,(2\psi_b)}}{C_{ox}} \tag{2.7}$$

The definitions of the other symbols are:

1) k is the Boltzmann's constant: $k = 1.38\times10^{-23}$ J/K,
2) T is the absolute temperature,
3) e is the electronic charge: $e = 1.60\times10^{-19}$ C,
4) N_a is the acceptor doping concentration of the substrate,
5) n_i is the intrinsic carrier concentration of the silicon,
6) ε_{si} is the dielectric constant of silicon: $\varepsilon_{si} = 1.03\times10^{-12}$ F/cm,
7) Q_{ss} is the fixed charge located in the oxide close to the oxide-silicon interface,

8) ε_{ox} is the dielectric constant of oxide: $\varepsilon_{ox} = 3.45\times10^{-12}$ F/cm, and

9) T_{ox} is the thickness of the gate oxide.

1.3. Source-drain resistance

The source and drain are not perfect conductors and have a resistance. The most common method to extract R_{sd} is to treat the MOSFET as an equivalent circuit comprising the source (R_s), drain (R_d) and channel (R_{ch}) resistances in series, where $R_{sd} = R_s + R_d$ which is illustrated in Figure 2.4, where the three capacitors, C_{gd}, C_{ds}, and C_{gs} represent the parasitic capacitances.

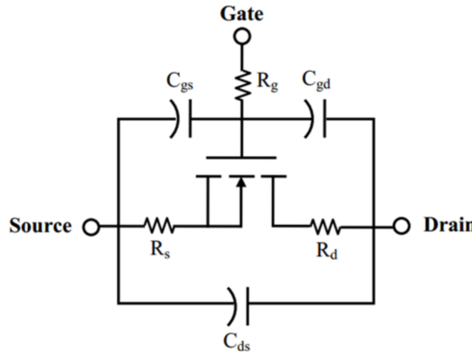

Figure 2.4 An equivalent circuit for n-type MOSFET showing the parasitic capacitances and resistances [13].

The resistance from drain to source of the MOSFET is determined by the property of the charged layer in the channel, and can be expressed as [12]:

$$\mathrm{R_{ch}} = \frac{L_g\, T_{ox}}{W_g\, \mu_{ch}\, \varepsilon_{ox}\, (V_{gs} - V_{th})} \tag{2.8}$$

where μ_{nch} is the carrier mobility in the channel, L_g is the gate length, and W_g *is the* gate width which are shown in Figure 2.1.

1.4. On-state current

The geometry of the MOSFET is different in the x, y and z directions as shown in Figure 2.1. To simplify the description of effects within a MOSFET, the gradual channel approximation is commonly made. This assumes that the electric field along the channel, E_x of the MOSFET is much smaller than the vertical electric field and enables the use of the one-dimensional form of Poisson's equation. Thus W_{dep} at a point x along the channel is

given by the potential at that point using the simple one-dimensional. This approximation is good if the gate/channel length L is larger than the W_{dep}.

Under the charge-sheet approximation, it is further assumed that all the inversion charges are confined at the semiconductor surface in a sheet, and there is no potential drop or band bending across the inversion layer [10]. Thus it can be written:

$$Q_{inv}(x) = C_{ox}(V_{gs} - V_{th} - V_{cs}(x)) \quad (2.9)$$

where $V_{cs}(x)$ is the channel potential with respect to the source. $V_{cs} = 0$ at the source and $V_{cs} = V_{ds}$ at the drain. x = 0 at the source end and equal to L, at the drain end.
The electron flow in the channel, or drain current, I_d is a drift current caused by E_x [8];

$$I_d = \frac{Q_{inv} W L}{t_r} \quad (2.10)$$

where W is the channel width and t_r the carrier transit time. If the velocity of the carriers is constant between the source and drain, the transit time equal [8];

$$t_r = \frac{L}{v} \quad (2.11)$$

where L the channel length, v the carrier velocity along the channel, is related to E_x by the carrier mobility, μ, which for now is assumed to be constant and independent of E_x [10]:

$$v = \mu E_x = \mu \frac{dV_{cs}(x)}{dx} \quad (2.12)$$

By combining equations (2.9)-(2.12):

$$I_d = C_{ox}\, \mu\, W \frac{dV_{cs}(V_{gs} - V_{th} - V_{cs}(x))}{dx} \quad (2.13)$$

By integrating from source (x = 0, $V_{cs}(0) = 0$) to drain (x = L, $V_{cs}(L) = V_{ds}$)

$$\int_0^L I_d dx = C_{ox}\, \mu W \int_0^{V_{ds}} (V_{gs} - V_{th} - V_{cs}(x))\, dV_{cs} \quad (2.14)$$

The drain current is constant along the channel and for $V_{ds} << V_{gs} - V_{th}$, the final expression for I_d is obtained [10]:

$$I_d = \mu \frac{W}{L} C_{ox} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (2.15)$$

This equation captures the basic on-state behaviour of a MOSFET, which starts at $V_{gs} \geq V_{th}$ and provided $0 < V_{ds} < V_{gs} - V_{th}$ the drain current increases linearly with V_{gs} since the quadratic term can be ignored [10]. This is called the linear region and is often simplified to:

$$I_d = \mu \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_{th} \right) V_{ds} \right] \qquad (2.16)$$

As V_{ds} is increased, I_d increases but Q_{inv} at the drain decreases (equation (2.9)) creating a non-uniform distribution of Q_{inv} along the channel. Once $V_{ds} = V_{gs}$-V_{th}, Q_{inv} at the drain end of the channel reaches zero, creating a region of high resistance, and the channel is said to be pinched off. Further increase in V_{ds} results in an extension of the pinch-off point towards the source and the extra potential is dropped across this increasing resistance. The drain current remains essentially constant and the MOSFET is said to be in the saturation region.

The saturation current, I_{dsat}, is given by:

$$I_{dsat} = \mu \frac{W}{L} C_{ox} \left(V_{gs} - V_{th} \right)^2 \quad \text{for } V_{ds} > V_{gs}\text{-}V_{th} \qquad (2.17)$$

The carrier mobility μ was introduced as the proportionality coefficient in the dependence of drift velocity on the applied electrical field as is defined in equation (2.12). This was assumed to be constant to convey the basic physics of MOSFET operation. μ is dependent on the effective mass of the carriers which is calculated from the band structure of the semiconductor. I_d is proportional to μ, higher μ corresponds to faster switching circuits [10].

1.5. Off-state current

This sort of leakage is undesirable because the current flowing through the device in the off-state device can cause the device failure, or RF noise [10]. Experimentally, Q_{inv} does not abruptly fall to zero when $V_{gs} \leq V_{th}$. The transition from full depletion to strong inversion is in fact more gradual as there are mobile carriers in the channel even for sub-threshold V_{gs}. Their concentration is very small and rapidly decays as V_{gs} is reduced below V_{th}. Nonetheless they account for the gradual decay of I_d from above threshold toward zero. The current I_d, which exists for $V_{gs} \leq V_{th}$ is known as the sub-threshold current and occurs when the channel is weakly inverted corresponding to $\psi_b < \psi_s < 2\psi_b$. The electrons have to overcome the potential barrier formed by the n+ source and p-substrate. The drain current I_d of a MOSFET

includes both drift and diffusion current components. When V_{gs} is lower than V_{th}, the I_d is low dominated by the diffusion current. This defines the subthreshold drain current given by:

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} (n-1) \left(\frac{KT}{e}\right)^2 e^{\frac{q(V_{gs}-V_{th})}{nkT}} (1 - e^{-eV_{ds}/KT}) \qquad (2.18)$$

When V_D is greater than a few kT/e, $\left(1 - e^{-\frac{eV_{ds}}{KT}}\right) \approx 1$. Then, the following is obtained:

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} (n-1) \left(\frac{KT}{e}\right)^2 e^{\frac{q(V_{gs}-V_{th})}{nkT}} \qquad (2.19)$$

It is apparent that the subthreshold drain current is independent of the drain-source voltage V_{ds}. It decreases exponentially with decreasing V_{gs}. The leakage current or off-state current (I_{off}) is normally defined as the drain to source current when V_{gs}= 0 and V_{ds}= V_{dd}. It is the drain current when no gate voltage is applied [3]. This off-state current is influenced by several other parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide, channel/surface doping profile and supply voltage (V_{dd}). It can be expected that I_{off} would increase by about 10 times for every 100-mV reduction of V_{th}.

The parameter n in Eqs. (1.18)-(1.19) is often termed body effect coefficient. It is typically
between 1- 1.4 and is calculated as:

$$I_D = 1 + \frac{\sqrt{\varepsilon_{Si}\, e\, N_{sub}/4\Psi_b}}{C_{ox}} \approx 1 + \frac{3t_{ox}}{W_{dn}} \qquad (2.20)$$

The parameter μ_{eff} in Eqs. (1.18) and (1.19) represents the effective mobility of the carriers in the inversion layer of the MOSFET. The electron and hole mobility in the inversion layer can be described by the following universal relations [14]:

$$\mu_{eff,n} = \frac{638}{1+(E_{eff}/7.10^5)^{1.69}} \qquad (2.21)$$

for the electron mobility, and

$$\mu_{eff,p} = \frac{240}{1+(E_{eff}/2.7\, .10^5)} \qquad (2.22)$$

for the hole mobility. E_{eff} is the effective electric field perpendicular to the channel direction. It can be seen that μ_{eff} decreases very rapidly with increasing E_{eff} at high E_{eff}.

When V_{gs} is higher than V_T, I_D is dominated by the drift current given by:

$$I_d = \frac{W}{L}\, \mu_{eff}\, C_{ox} \left[(V_{gs} - V_{th})V_{ds} - nV_{ds}{}^2/2 \right] \quad (2.23)$$

The I_D-V_{ds} characteristics for an n-MOSFET with V_{gs}>V_{th} are shown in Figure 2.5. At small drain voltage ($V_{ds} < (V_{gs} - V_{th})$) which shown in Figure 2.6, MOSFET device operates in the linear regime the relation $mV_{ds}{}^2/2$ can be neglected. The drain current I_D in the linear regime can be expressed as:

$$I_d = \frac{W}{L}\, \mu_{eff}\, C_{ox}\, (V_{gs} - V_{th})V_{ds} \quad (2.24)$$

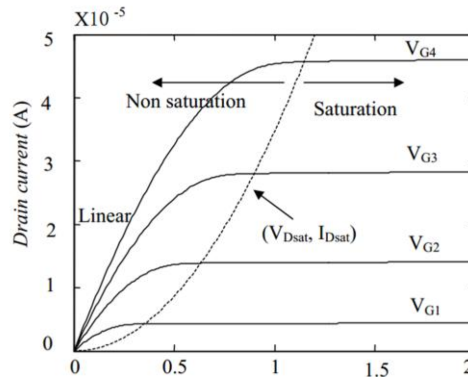

Figure 2.4 I_D-V_{ds} characteristics for an n-MOSFET with

V_{G4}>V_{G3}>V_{G2}>V_{G1}>V_T [15]

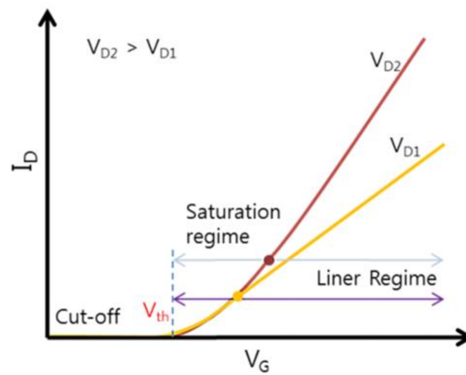

Figure 2.5 FET operation schemes in transfer (I_D-V_G) characteristics [15].

At linear regime, MOSFET operates as a gate controlled resistance.

When the V_{ds} is increased further, the increase of I_D follows a parabolic behaviour as described in Eq. (1.19), until a maximum or saturation value is reached. This occurs when:

$$V_{ds,sat} = (V_{gs} - V_{th})/n \quad (2.25)$$

at which

$$I_d = I_{d,sat} = \frac{W}{L}\, \mu_{eff}\, C_{ox}\, \frac{(V_{gs}-V_{th})^2}{2n} \tag{2.26}$$

Above $V_{d,sat}$, I_d stays constant at $I_{d,sat}$, independent of V_{ds} [15].

$$I_d = \mu\ C_{ox}\, \frac{W}{L}(n-1)\ \left(\frac{KT}{e}\right)^2 e^{e(V_{gs}-V_{th})/nKT}\left(1-e^{-eV_{ds}/KT}\right) \tag{2.27}$$

where $n = 1 + C_{dep}/C_{ox}$

A plot of $\ln(I_d)$ as a function V_{gs} gives a linear behaviour in the sub-threshold regime. The reciprocal slope of this line is known as the sub-threshold slope (SS), which is a measure of the efficacy of V_{gs} in modulating I_d. A small sub-threshold slope (steep transition from off-state to on-state) is desirable for the ease of switching the transistor current off. For a very small V_{gs}, the sub-threshold current is reduced to the leakage current of the source/drain junctions. This determines the off-state leakage current and therefore the standby power dissipation in CMOS circuits.

1.6. Transconductance

Transconductance is a measure of how fast the transistor is able to switch while sweeping the gate voltage, and it is related to the gain of the transistor. It is given by the ratio of the change in drain current to the change in gate voltage at a constant drain-source bias. The transconductance is a measure of the sensitivity to surface charges [10]. A high transconductance value means a bigger change in drain current for a given change in surface charge which translates to higher device sensitivities. For that reason, the maximum transconductance gate voltage is sometimes chosen as the operating point for sensor measurements. High maximum transconductance values > 10 µS were found for all devices, (Figure 2.6, right axis) [16].

The transconductance is defined as the derivative of Eq. (1.22) with respect to V_{gs}:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{W}{L}\ C_{ox}\ \frac{\mu_0}{[1+\theta(V_{gs}-V_{th})]^2} V_{ds} \tag{2.28}$$

The threshold voltage extraction using the linear extrapolation method for a short channel device operated in the linear region as shown in Figure 2.6. The intercept point with X-axis indicates the threshold voltage [17]. The slope of the line yields the mobility. However, this method is sensitive to the mobility degradation and series resistance. The

maximum slope of g_m usually lies in the non-linear tail of the I_d-V_{gs} curve. Thus, this method tends to obtain a value of V_t closer to the point where I_d becomes negligibly small.

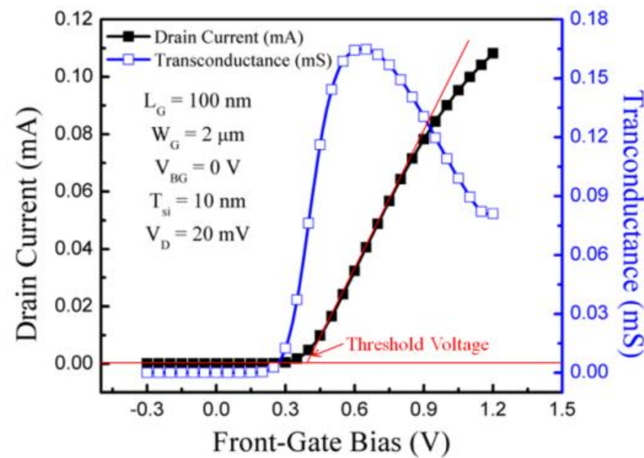

Figure 2.6 Experimental drain current and transconductance curves as a function of front-gate bias showing the linear extrapolation method for threshold voltage. N-channel SOI MOSFET with L_G = 100 nm and T_{si} = 10 nm [18].

From Eq. 2.24, if μ_{eff} is constant, the transconductance g_m can be calculated as:

$$g_m = \frac{\partial I_D}{\partial V_G} \Big|_{V_d=Const} = \frac{W}{L}\, \mu_{eff}\, C_{ox}\, V_D \qquad (2.29)$$

I_D increases linearly with V_{ds}.

1.7. Subthreshold slope

One of the most well-known feature of a FET device is the semi-logarithmic plot of the drain current I_d as a function of the gate voltage V_{gs}, called $I_d(V_{gs})$ transfer characteristic, as illustrated in Figure 2.7 [15].

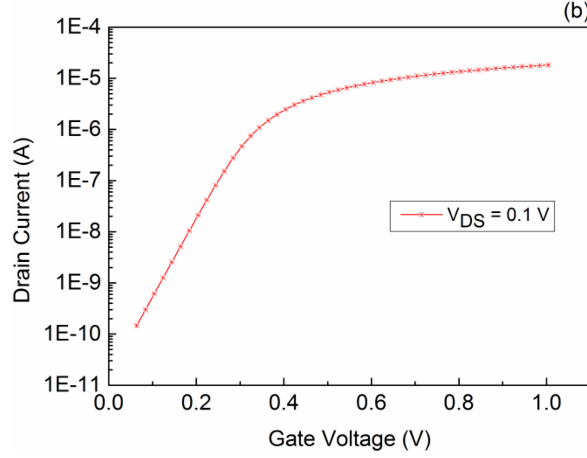

Figure 2.7 log scale (b) of simulation drain current (I_{DS}) versus gate voltage (V_{gs}) for TG FinFET device [19].

For $V_{gs} < V_{th}$, one can define the subthreshold region, a region of particular interest for sensing applications. An explicit expression for the I_d in the subthreshold region for a double-gate thin-film is provided in [20]:

$$I_d = \frac{W}{L}\mu_n 4\, C_{Si}\left(\frac{KT}{q}\right)^2\left(1 - e^{\left(-\frac{q}{KT}\right)\left(\frac{Q_D}{8C_{Si}}\right)}\right).\left[1 - e^{-\left(\frac{qV_{ds}}{KT}\right)}\right].e^{q/KT\left(V_{gs}-V_{FB}-\left[\frac{\frac{Q_D}{2}}{C_{ox}}\right]-2\Phi_f\right)} \quad (2.30)$$

where μ_n is the electron mobility, $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the capacitance per unit area associated to the silicon film, V_{ds} and V_{gs} the voltage at the drain and gate contacts. The variation of the I_d current according to V_{gs} in the subthreshold region is expressed by the subthreshold slope (inverse or the real slope of $I_d(V_{gs})$), defined as:

$$SS = \frac{\delta V_{gs}}{\delta(\log I_d)} = \frac{\delta V_{gs}}{\delta \Phi_S}.\frac{\delta \Phi_S}{\delta(\log I_d)} \quad (2.31)$$

Where $\frac{\delta V_g}{\delta \Phi_S}$ is called body m-factor and it describes the coupling between the gate and the surface potential, while $\frac{\delta \Phi_S}{\delta(\log I_d)}$, known as n-factor, is limited to a minimum value according to the Fermi-Dirac distribution. For a bulk MOSFET the subthreshold slope can further be expressed as:

$$SS = n.m = \frac{KT}{q}\ln(10)\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) = 59\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) mV/dec \quad (2.32)$$

where C_D and C_{it} are the capacitances associated to the depletion region and the interface trap states, respectively. The subthreshold slope is constant and independent from the drain and

gate voltage. An ideal FET device has a subthreshold slope of SS_0 = 59 mV/dec at room temperature (300 K) [19]. The full-depletion condition allows thin-film to get closer to the ideal value. In first approximation, the variation of the depletion charge with the front gate is, in fact, $\delta Q_D/\delta V_{gs} = 0$, meaning that $C_D \approx 0$ and the subthreshold slope approaches its theoretical limit [21] with m = 1:

$$SS \cong \frac{KT}{q}\ln(10) \equiv SS_0 \tag{2.33}$$

which is valid for small thicknesses ($t_{Si} < x_{dmax}$) [22] and neglecting the interface traps. Under scaling, the subthreshold slope of a thin-film device with the same parameters of a bulk device or thick-film will be steeper. In turns, in the subthreshold regime any variation of gate voltage δV_{gs} is perfectly coupled to the surface potential φ_S, giving rise to an equal increase. In a real device, the theoretical limit is never reached due to the presence of traps at the Si-Oxide interface.

1.8. Drain induced barrier lowering (DIBL)

DIBL is one of the most important short channel effect parameter of nanoscale FET device structures, since it estimates the overall gate control of the device on the channel electrostatics of the device. The effect of DIBL is to reduce the threshold voltage in nanoscale MOS devices thanks to the modulation of the source to drain channel potential barrier by the drain voltage. This makes the conduction of device channel available for smaller gate voltages [23]. The DIBL is defined as the ratio of the difference in threshold voltage measured at a low value to high value of the drain voltage. The drain induced barrier lowering is defined as the ratio of change in threshold voltage ΔV_{th} to change in drain voltage ΔV_{ds} [24].

$$\text{DIBL (mV/V)} = \frac{\Delta V_{Th}}{\Delta V_{DS}} \tag{2.34}$$

DIBL is more prominent at high drain voltages and shorter channel lengths. We can reduce drain induced barrier lowering effect by using higher surface and channel doping [24, 25]. For a short channel device, V_{DS} lowers the potential barrier between source and channel, which is named drain-induced barrier lowering (DIBL) as shown in Figure 2.8.

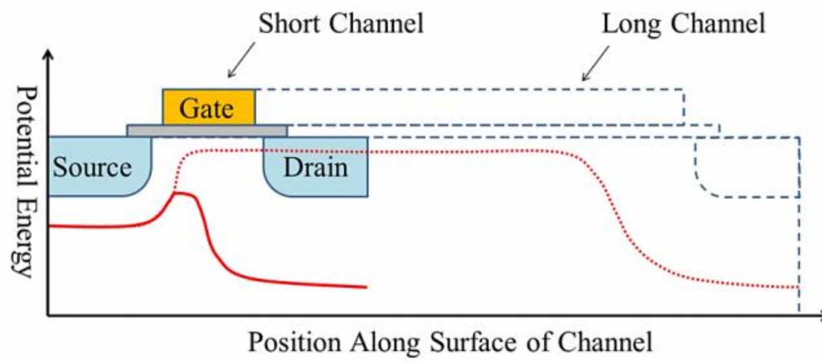

Figure 2.8 Drain-induced barrier lowering in short channel device. Drain is biased and it pulls down the potential energy around drain [18].

This effect limits the maximum operation voltage of device [26]. To avoid DIBL, the enhancement of gate control or the separation of merged depletion region is needed. Thus, increase of substrate doping level, delta doping into the substrate and the so-called pocket or halo implant, has been used in typical planar devices [27-28].

1.9. Mobility

Carrier mobility is considered as an attractive concept over the years in industry and research. However, mobility and its properties are generally investigated in the context of planar structures and doping levels, crystal quality, electric fields, and temperature [29, 30]. Exciting thesis research topics let the researchers focus on carrier mobility on crystal orientations other than the most frequently used (100)-oriented silicon surface.

Carrier mobility represents how quickly carriers can move in the material. When an electric field E is applied across the material, the carriers acquire a velocity in the field direction. This velocity is superimposed to the random thermal induced motion. An average velocity, named drift velocity v, may be used to describe the ensemble movement of the carriers:

$$v = \mu \cdot E \tag{2.35}$$

where μ is the carrier mobility. In case of very intense electric field the velocity saturates [18];

Each mobility source has different temperature dependences; they can be identified by low temperature measurement. Jeon et al. and Takagi et al. showed the temperature dependence of each scattering mechanism using experimental mobility analysis [31, 32].

2. The Silicon FET as a Nanoelectronic Device

2.1. What is Nanotechnology ?

Nanotechnology has been defined as work at the scale range 1 to 100 nm lengths to produce structures, devices, and systems that have novel properties because of their nanoscale dimensions **[33]**. Within this nanoscale regime, new phenomena occur (caused, for example, by the dominance of interfaces and quantum mechanical effects). These new phenomena may be exploited to improve the performance of materials, devices, and systems. Nanotechnologies also involve the manipulation and control of matter at the nanoscale. The top-down methods for processing of nanostructured materials involve starting with lithography/etching a bulk solid and then obtaining a nanostructure by structural decomposition. In the current day, silicon technology meets the definition of nanoelectronics very well and that unconventional technologies could play an important role in future electronic system by complementing the capabilities of nanoscale silicon technology, rather than by attempting to replace it [34].

2.2. Silicon material

Silicon has formed the basis material of the semiconductor industry, almost since its birth and has remained the material of choice since it superseded germanium, which was used to make the first transistors. Silicon has the advantages of being easily obtainable (comprising a quarter of the Earth's crust), therefore inexpensive. It has good physical properties that allow easy definition of complex device structures. Lastly its oxide is a very good electrical insulator and, unlike that of germanium, is insoluble in water which reduces processing complexity. These factors combine to provide a cheap platform on which to fabricate reliable FinFETs [8].

It is known that 21st-century silicon technology has evolved into a true nanotechnology which is already below 100 nm. The materials used in these silicon devices have properties very different from that of the bulk materials. Nanoscale silicon transistors have higher leakage current, lower drive current, and exhibit more variability from device to device. New circuits and architectures will need to be developed to accommodate such devices. It matters little whether the material is silicon or something else; the same issues face any nanoelectronics technology. It is likely that many of the advances and breakthroughs at the circuits and systems levels that will be needed to make nanoelectronics successful will come from the silicon design community [34].

The importance of developing and understanding of how engineering *devices* operate at the nanoscale is a good reason to support nanoscience research. Another reason is that devices to complement silicon technology might be discovered. Therefore, research on nanoelectronics will prove to be a good investment for several reasons [34].

Accelerating the development and successful of nanoelectronics will require a partnership between science and engineering. It was the same for semiconductor technology. The scientific community developed the understanding of semiconductor materials and physics and the engineering community used this base to learn how to design devices, circuits, and systems. Figure 2.9 summarizes this partnership. Science works in the nanoworld with individual atoms, molecules, nanoscale structures and devices, and assembly processes. Systems engineers work in the macroworld on complex systems with terascale device densities [34].

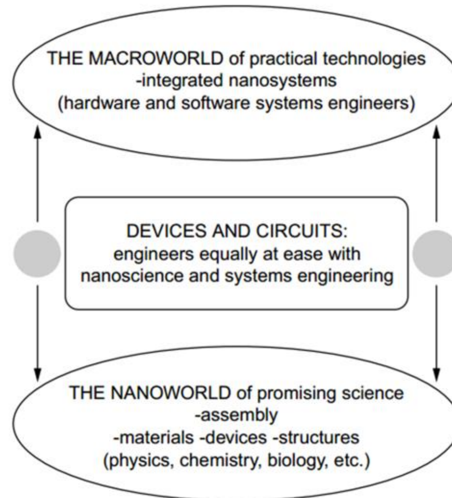

Figure 2.9 Science, engineering, and nanoelectronics [34].

In the middle are the device and circuit engineers. This section needs to learn how to think and work at the nanoscale to build devices and circuits that can connect to the macroworld. This job is to hide the complexity of the nanoscale device by packaging it in a form that systems engineers can use (e.g., a compact circuit model). To turn the promise of nanoscience into practical technologies, it is essential that the systems engineering community be engaged in the effort [34].

2.3. Silicon FETs in the Nanometer Regime

Nanoscale device technology is a current topic of research for all the production companies, like TSMC, Intel, and Samsung, which are in the race to get a high performance of microprocessors beyond the barrier of 14 nm. The International Technology Roadmap for Semiconductors (ITRS) looking for get 9-nm physical gate lengths for integrated circuit (IC) transistors in 2016 [35]. At the same time, major IC manufacturers have reported transistors with 10-nm (or shorter) gate lengths on IEDM 2002 [36, 37], which demonstrate the promise of pushing IC technology to the 10-nm regime. To scale silicon transistors down to the 10-nm scale, new device structures are needed to suppress the short channel effects such as subthreshold voltage (SS), Drain Induced Barrier Lowering (DIBL), and high leakage current (I_{off}) [38]. Figure 2.10 shows a schematic illustration of a fully depleted, double-gate (DG) MOSFET; this device offers good prospects for scaling silicon transistors to their limits [39]. Other approaches (e.g., the FinFET [36] and the tri-gate MOSFET [40]) are also being explored. At a 9-nm gate length, acceptable short-channel effects require a fully depleted

silicon body thickness of 3 nm or less, and an equivalent gate oxide thickness of less than 1 nm. At such dimensions, the properties of the silicon material will be affected by quantum confinement (e.g., the bandgap will increase), and device properties will be influenced by quantum transport.

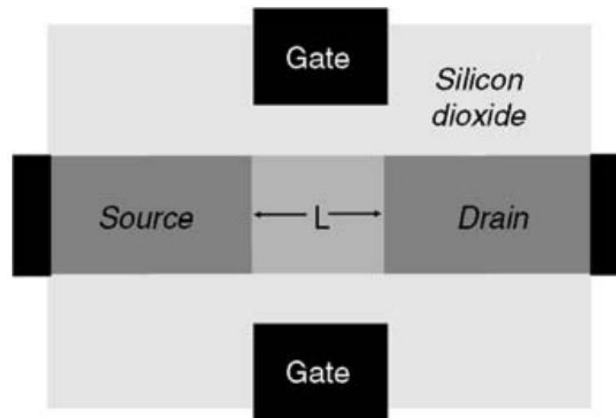

Figure 2.10 The double-gate MOSFET structure [34].

Traditional device equations are based on the drift-diffusion theory [38], which assumes that the device scale is much larger than the electron wavelength (~ 8 nm at room temperature) and the electron mean free-path (the average distance an electron travels between two collisions, ~ 10nm for electrons in the inversion layer). The first assumption allows the researchers to treat electrons as classical particles with zero size, and the second one justifies the “local transport” property (the electron velocity at a position is solely determined by the local electric field and mobility). Unfortunately, at the nanoscale, neither of these assumptions is well satisfied. As a result, to capture the new physical effects that occur at the nanoscale, the old device theory must be modified or even completely replaced by a new quantum transport theory. Four important phenomena need to be properly treated in the modelling of nanotransistors [34]:

1. Quantum confinement
2. Gate tunneling
3. Quasi-ballistic transport
4. Source-to-drain (S/D) tunneling

The first two effects occur in the confinement direction (normal to the gate electrode(s)) of the FET device. As silicon technology entered the sub-100-nm regime (the corresponding oxide thickness <3nm), those effects became significant and began to affect

the FET device threshold voltage and leakage currents in the "Off-state". In contrast to the quantum confinement and gate tunneling, quasi-ballistic transport, the source-to-drain tunneling begin to significantly affect the device performance of the silicon FET transistor when the gate length scales down to 10 nm or less [41]. Therefore, the exploration of these microscopic transport effects is important for the description of silicon FinFETs at their scaling limit, as well as the understanding of device physics of other nanoscale devices [34].

2.4. The short channel effect

The short channel effect is the decrease of the device threshold voltage as the channel length is reduced. This is important as it is hard to control channel lengths precisely due to process tolerances. Statistical variations in channel lengths then lead to problems with V_{th} control [42].

Providing the channel is sufficiently long, the source and drain depletion regions only occupy a small fraction of the entire channel and V_{gs} controls essentially all of the depletion charge. Thus the MOSFET can be abruptly switched off. As the channel length decreases, the fraction of charge controlled by the gate decreases. Less gate charge is now required to invert the channel, resulting in a lower V_{th}. With increasing V_{ds}, the reverse-biased depletion region at the drain extends further into the channel area and the gate controls even less depletion charge, further lowering V_{th}. When V_{ds} is sufficiently high or channel length sufficiently short, the drain depletion region merges with the source depletion region. Thus the source-channel potential barrier is lowered below the built in potential resulting in significant drain leakage current with the gate unable to shut it off. Control of the channel by the gate can be retained by not only increasing C_{ox} but by proper scaling down of the source and drain junction depths and scaling up of the substrate doping concentration. Increasing the doping concentration reduces the depletion region widths; however, the carrier mobility is degraded due to increased number of ionized impurities and increased vertical electric field. In addition, V_{th} is increased. If the source and drain junction depths were equal to the inversion layer thickness, the gate would retain complete control of the channel. Achieving such ultra-shallow junctions is limited by diffusion of the source and drain dopants [8].

2.5. Channel control

The electrostatics of the device channel can be controlled much more effectively by using multiple gates than in the FDSOI MOSFET, allowing for further scaling. The basic principle is shown in Figure 2.11 which shows how the addition of a second gate further

suppresses the source and drain depletion regions. This notion has given birth to a host of three-dimensional multi-gate MOSFETs which include a range of double-gate, triple-gate, and surrounding-gate MOSFETs, with the latter theoretically providing the best possible control of the channel region.

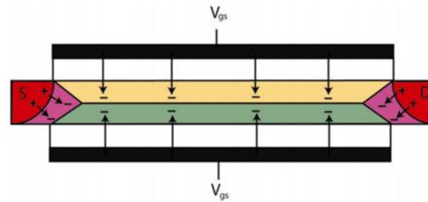

Figure 2.11 Cross section of a fully depleted double-gate MOSFET. The electric fields (arrows) and corresponding depletion charges from both gates and the source and drain are shown [8].

2.6. Multi-gate transistors

Various innovative device structures have been proposed by researchers to address the above mentioned challenges and continue device scaling. In these transistors, the channel is surrounded by multiple gates, allowing better control of the channel and thus yielding more effective suppression of leakage current. Multi-gate transistors also have higher on-current (I_{on}), which leads to better device performance [43]. Among various multi-gate transistors, double-gate field-effect transistors (DGFETs) have gained popularity owing to ease of fabrication and better yield [44]. The presence of the second gate helps a DGFET to reduce drain influence on the channel and thus reduce short-channel effects such as DIBL and degraded subthreshold slope (SS).

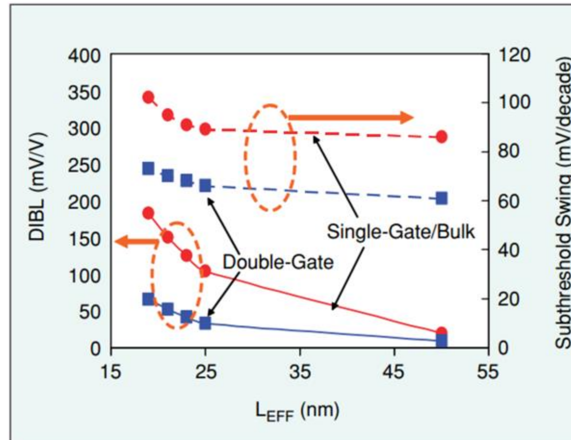

Figure 2.12 DIBL and subthreshold swing versus effective channel length for DG and bulk-silicon nFETs. The DG device is designed with an undoped body and a near-mid-gap gate material [45].

Figure 2.12 compares DIBL and SS of a conventional device and a DGFET based on MEDICI (device simulator) predicted data at various effective channel lengths (L_{EFF}) [45]. It can be seen that both the DIBL and subthreshold swing are improved by using the double gate structure. Thus, a DGFET enables scaling to the 22 nm technology node and beyond. Figure 2.13 not only shows reduced off-current (I_{off}), but also demonstrates an improved I_{on}/I_{off} ratio.

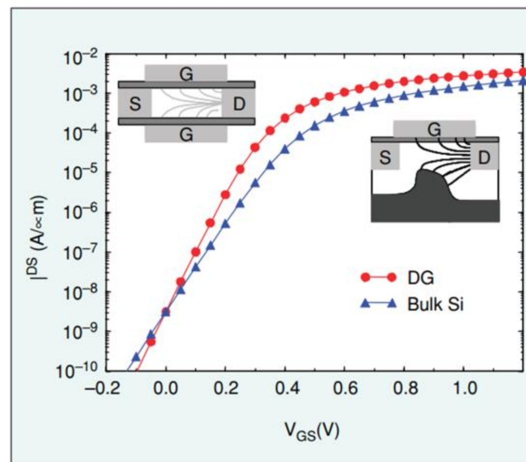

Figure 2.13 I_{DS}-V_{GS} characteristics on log scale for DGFETs and bulk-silicon transistors at equalized subthreshold current [45].

Figure 2.14 shows three major types of DGFETs. Type I augments a conventional FET with a second gate buried in the body itself. In Type II, the silicon body is rotated to a vertical orientation with drain/source sitting at the top/bottom. In Type III, the silicon body is made to stand up with source/drain being on either side of the channel. Type III is popularly known as FinFET. Some major challenges in fabricating DGFETs are maintaining an identical size for both the gates, alignment of the gates, alignment of source/drain to the gates, and connecting both gates in an area-efficient manner. FinFETs address these fabrication concerns and, hence, have emerged as the most promising DGFET [46].

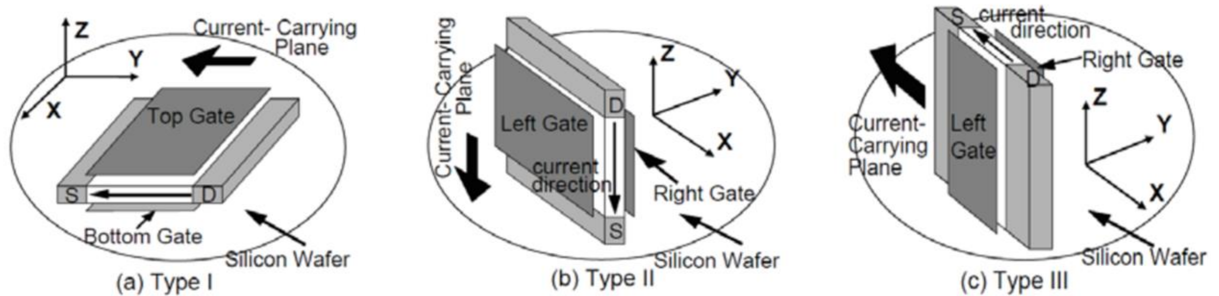

Figure 2.14 Different kinds of DGFETs [46].

Beyond the tri-gate FinFET, Gate-All-Around (GAA) will be the optimized gate structure in 3D multi gate MOSFETs. GAA FET has gate electrodes wrapped around the channel region. Extremely narrow nanowire channel body has pseudo-1D channel structure. The short channel effect immunity of nanowire FET can be quantitatively analyzed by using natural length λ which can be derived from Poisson's equation (Table 2.1) [2].

Single Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{si} t_{ox}}$
Double Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$
Triple Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{3\varepsilon_{ox}} t_{si} t_{ox}}$
Gate-All-Around	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{8\varepsilon_{ox}} t_{si}^2 \ln\left(1 + \frac{2\, t_{ox}}{t_{si}}\right) + \frac{t_{si}^2}{16}}$

Table 2.1 Natural length of devices depending on different gate structures [2].

The natural length is the length of the channel region controlled by the drain. It means that the smaller λ, the smaller short channel effect can be driven in given device structures. To be free of short channel effects, λ should be at least 5 times shorter than the effective gate length. From the equation of λ with single, double, and triple gates, it can be simply guessed that approximately the value of λ can be estimated by division with the square root of gates number. Because the smaller λ can reduce the short channel effects, the device has good immunity from increased gate number. Moreover, from these equations, it should be notable that the reduction of t_{ox} decreases short channel effects. Decreasing t_{ox} has a limitation due to the tunneling current leakages below 1.5 nm gate oxide thickness. Thus high-k gate dielectric can effectively reduce λ. The effect of t_{si} thinning is also essential to decrease λ and short channel effects. A quantum confinement induced by t_{si} reduction enhances the volume inversion effect and yield the increase of V_{th}. However, ultra-thin body raises the mobility degradation even though the reduction of t_{si} can decrease short channel effects [47].

2.6.1. FinFETs technology

FinFET has been considered as an attractive candidate for advanced CMOS technology node applications. This nonplanar double-gate transistor has emerged as most viable alternative [2, 45] owing to low subthreshold leakage, superior gate control over the channel, and reduced sensitivity to process variations. Initially, the cost and complexity associated with fabrication were the primary challenges in making these devices the industry driver. These are no longer critical as the key players in the semiconductor industry have

managed to fabricate these devices at roughly the same cost and with minor modifications to the conventional CMOS fabrication process. Superior performance, significantly lower leakage, and low fabrication cost are the main reasons behind recent adoption of these devices by various companies. Intel was the first company to introduce FinFET technology into mass production, in 2011, and reported that the manufacturing cost is comparable to that of the conventional planar MOSFET technology, higher by only a low single-digit percent. It also reported that no special manufacturing equipment is required [48]. TSMC has announced availability of 14nm FinFET chips on 450mm wafers by 2016 [49]. Samsung had demonstrated a functional FinFET based SRAM as far back as 2005 [50]. A fully functional chip consisting of 3000 FinFETs was fabricated by Infineon in 2006 [51]. Major industry players like IBM, Globalfoundries, Toshiba, and NEC joined to design the smallest area (0.063 square micron) FinFET based SRAM using optical lithography at the 22 nm technology node [52]. They demonstrated such an operational SRAM at 0.4V. Intel, another semiconductor giant, has taken a different route by introducing a tri-gate FET (a variant of FinFET) at the 22 nm technology node. Intel was the first company to manufacture products, which basically have their applications in computers and servers at the 22 nm tri-gate FinFET technology and currently is looking to grow at a high rate in future with the market of the 7 nm FinFET technology. FinFET is one of the most attractive devices for implementing nanoscale CMOS technology which gives improvement on electrical and physical design convergence at advanced nodes such as the products of CPU, SoC, FPGA, MCU, and network processor. Clearly, all major players in the semiconductor industry have accepted FinFETs as the prime workhorse to continue scaling in the upcoming decade. Hence, our focus in this thesis is to investigate this device in depth, identify potential challenges, and try to address them through novel solutions.

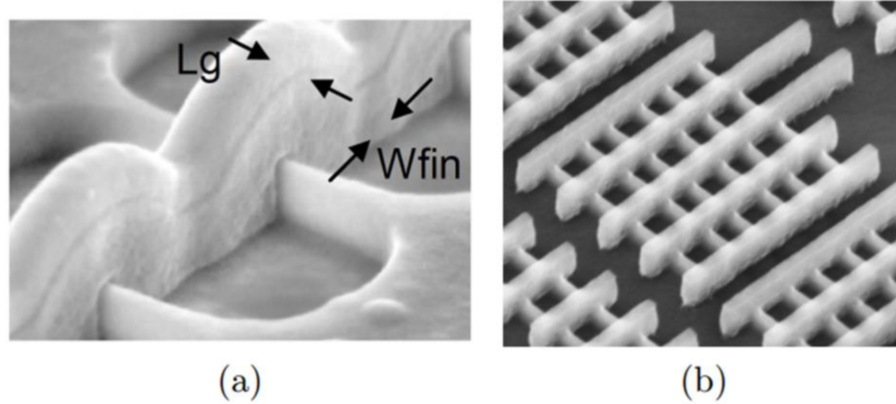

Figure 2.15 FinFET SEM photos. (a) Fabricated FinFET. (b) [53].

A FinFET can have multiple fins in parallel, all straddled by a single gate line, thus its effective width is given by;

$$W_{eff} = n(2H_{fin} + W_{fin}) \qquad (2.36)$$

where n is the number of fins, H_{fin} and W_{fin} is the fin height and width respectively. Adequate suppression of the short channel effect and off-state leakage current requires that $W_{fin} \sim L/2$. It is desirable for H_{fin} to be as large as possible to maximize W_{eff}, therefore I_d. Thus for the 22 nm node and beyond, the FinFET can essentially be treated as a fully depleted double gate device where I_d flows predominantly along its sidewall surfaces. Due to their vertical nature, a FinFET's sidewalls and top surface lie in the (110) and (100) planes respectively when the device is oriented parallel or perpendicular to the wafer flat of a standard (100) wafer. I_d therefore flows along the <110> direction. In this orientation, the hole mobility is maximized but the electron mobility is minimized. The electron mobility could be maximized by rotating the fins 45° as then the sidewalls would be in a (100) plane. However this incurs an area penalty on the wafer and increases complexity in circuit design, making it an unlikely option in VLSI circuits.

2.6.2. Silicon on insulator (SOI) technology

The use of SOI material makes the fabrication of multiple gate devices easier. Different kinds of transistors are developed such as: double gate [54], triple gate [55], FinFET [56] or gate all around [57]. Those architectures are summarized on Figure 2.16.

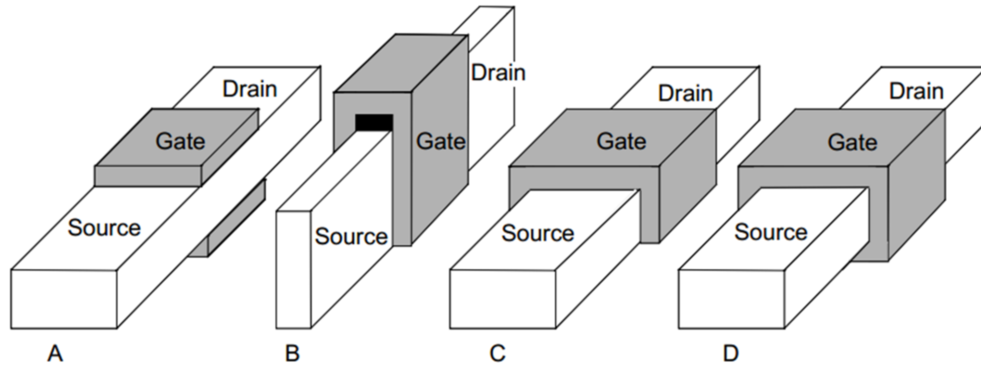

Figure 2.16 Scheme of multiple gate SOI devices. Planar double gate (a) FinFET, (b) triple gate, (c) quadruple gate, or (d) gate all around [34].

Two, three, or four gates are used to control the channel regions, leading to an increase of the electric field induced by the gate. With multiple gates, the transverse electric field (i.e., gate-to-channel electric field) is reinforced compared to lateral electric field (i.e., source-to-drain electric field). The main purpose of these architectures is to:

- Improve the scaling of the transistors (i.e., by limiting DIBL and short channel effects for a given drive current) for gate length below 50 nm
- Achieve levels of performance that are as good as classical planar CMOS devices.

With the improved performances achieved by those multiple gate SOI devices, we can imagine:

1. Having a lower I_{off} for a given V_{th} criterion of a bulk transistor, possibly thanks to its steeper subthreshold swing
2. Having a lower gate tunneling current
3. Having smaller performance variations, with the combination of intrinsic devices and metal gate material

SOI-based FinFETs offer excellent circuit operation due to easier leakage control, better performance, less variability, and lower cost. In an SOI FinFET, a metal gate wraps around an upright thin silicon fin with an insulating base and a thick spacer material at the top that separates the fin from the gate as is shown in Figure 2.16. In tri-gate transistors, the fin can be controlled from all three sides of the device (the top spacer is removed). The use of three gates surrounding the fin ensures an excellent electrostatic control [55]. The smaller fin

thickness (T_{si}) compared to gate length (L_g) ensures tighter control of the channel. The device channel is undoped or lightly doped to eliminate random dopant fluctuations caused by within-die process variations. FinFET functionality follows similar device physics as conventional MOSFETs. The effective width of a FinFET device is $2nH_{FIN}$, where n is the number of fins and H_{FIN} is the fin height. The transistor width can be increased to increase I_{on} by simply adding more fins to the structure (Figure 2.18). However, such a structure leads to width quantization that affects functionality, performance, and power, which are sensitive to the β ratio [58].

FinFETs device can be operated in two different modes: SG and IG (Figure 2.19). In the SG mode of operation, the front and back gates are shorted and biased together to switch the device on/off, providing maximum gate drive. In the IG mode of operation, the front and back gates are made independent by etching away the top part of the FinFET, thus, allowing them to be independently biased. This flexibility allows a designer to use a back-gate bias to alter the V_{th} of the front gate, hence, providing a better way to control I_{off}. The back gate of an IG FinFET can be forward (reverse) biased to dynamically increase (decrease) its I_{on} (I_{off}). However, its I_{on} is still far inferior to the I_{on} of an SG FinFET [59].

There are two distinct orientations for the Fins: (100) and (110). The channel surfaces of a FinFET lie in the (110) crystallographic plane when the fin is oriented parallel or perpendicular to the wafer flat or notch of a standard (100) wafer. Owing to carrier mobility anisotropy in crystalline silicon [60], the (100) plane maximizes electron mobility, whereas the (110) plane yields maximum hole mobility. This aspect can be exploited to make fast FinFET logic gates. However, as can be seen from Figure 2.18, such a non-systematic fin arrangement results in yield issues for sub-wavelength lithography [61].

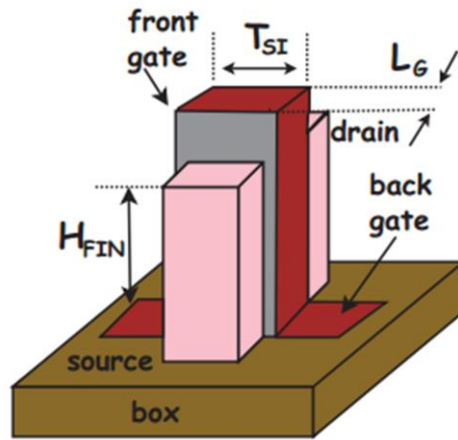

Figure 2.17 A typical n/p-FinFET device [59]

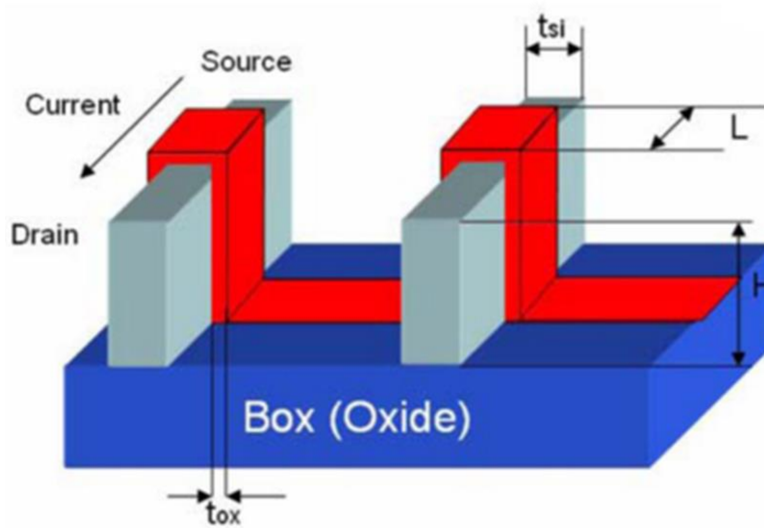

Figure 2.18 A multiple-fin FinFET structure [59].

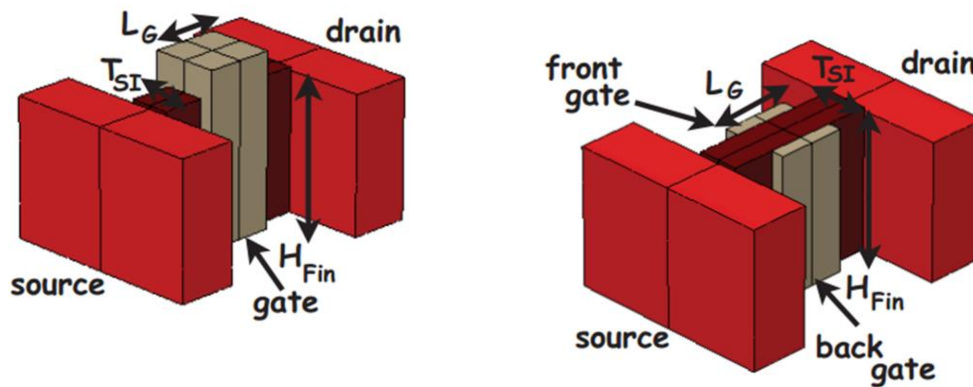

Figure 2.19 FinFET structures: (a) SG and (b) IG [59].

As long as the fin thickness (body thickness), T_{si}, is smaller than L_g, the short-channel effects are well suppressed and the subthreshold slope is basically the theoretical best case, approximately 62 mV per decade at room temperature. A new scaling path was born: L_g can be scaled by scaling the fin (body) thickness. If lithography and etching can produce 5 nm L_g, for example, they can produce approximately 5 nm T_{si}. Therefore, the condition $T_{si} \leq L_g$ can always be satisfied. In 1999, 18 and 45 nm working FinFETs and 10 nm FinFET simulation results were reported **[62]**. Soon after, 10 and then 5 nm FinFETs **[63]** were reported by IC manufacturers.

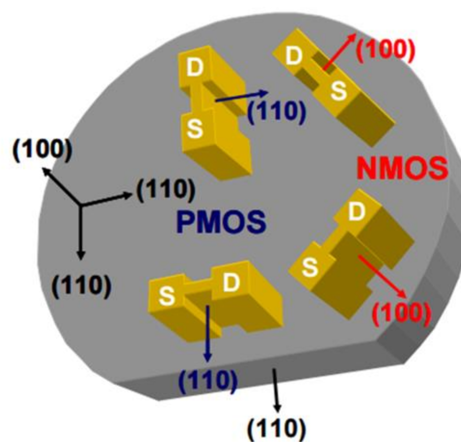

Figure 2.20 Oriented FinFETs with nFinFETs along 100 sidewalls and pFinFETs along 110 sidewalls [61].

When FinFET parameters may assume different values as gate underlap (L_{UN}), gate work function (Φ_m), and source/drain doping (N_{SD}). These devices are called asymmetric. These parameters assume the same value within a symmetric FinFET. It could be classify asymmetric FinFETs as single-parameter or multi-parameter asymmetric. In single-parameter asymmetric devices, only one of the parameters takes different values, whereas in multi-parameter asymmetric devices, more than one parameter take non-identical values. So far, researchers have primarily explored FinFETs with just one of the several parameters being asymmetric, e.g., asymmetric gate work function SG (AWSG) [64], asymmetric doping SG (ADSG) [65], asymmetric gate underlap SG (AUSG) [66], and asymmetric oxide IG (AOIG) [67] FinFETs. Logic gates based on AWSG FinFETs, which are considered much better placed in the leakage-delay spectrum relative to SG and IG devices, have shown promise in power/performance optimization of flip-flops, latches, and SRAMs [68]. However, ADSG and AUSG FinFETs have only been explored in the context of SRAM cell design.

2.6.3. ULTRA-THIN-BODY FET

In 1996, Chenming Hu and his research team proposed two implementations of the thin-body concept. They are the FinFET and ultrathin body (UTB). While the FinFET is now the mainstream advanced technology, examining a FinFET together with UTB puts the FinFET in perspective. A FinFET's ability to suppress the short-channel effects does not arise from it being three-dimensional, although that gives the FinFET an advantage in layout density. It arises from having a thin body that precludes the presence of a semiconductor (potential leakage paths) that is not very close to the gate. Reducing the silicon film thickness or silicon doping concentration from partially to fully deleted SOI (e.g., from 40 to 15 nm) would not improve the short-channel effects and may worsen them by eliminating the ground plane effect provided by the undepleted silicon body [69]. However, if the silicon film is only several nanometers thick as shown in Figure 2.21, short-channel effects can be greatly suppressed [70] by eliminating the worst leakage paths.

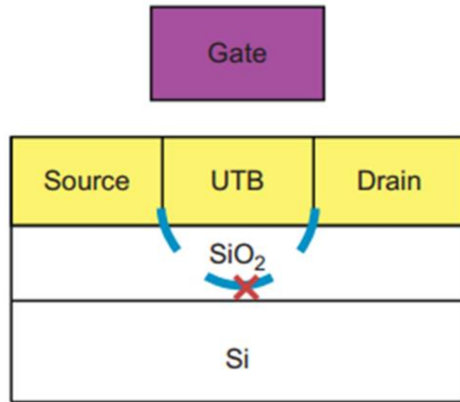

Figure 2.21 Ultrathin body (UTB) has no vulnerable leakage paths if silicon exists only within a few nanometers from the gate [71].

Figure 2.22 illustrates a log scale of I-V characteristics of UTB: simulated leakage current is reduced by approximately 10 times for every 1 nm drop of the body thickness in the UTB regime. The current implementation of UTB requires SOI substrates with silicon film uniformity of ±0.5 nm, or less than two silicon atoms, so that a 5 nm ultrathin silicon film will not have more than ±10% nonuniformity. In the future, two-dimensional semiconductors such as graphene, WSe_2, or MoS_2 may provide the ultimate singlemolecule thin body for UTB transistors.

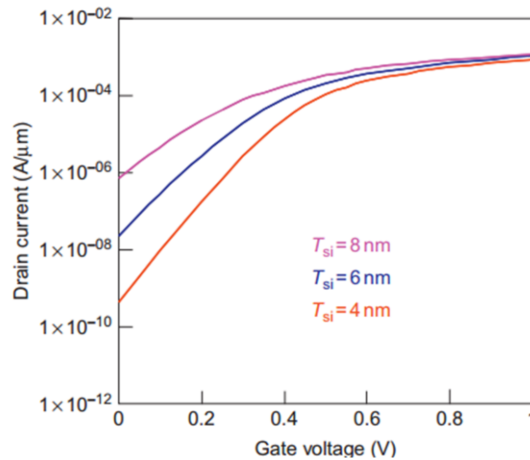

Figure 2.21 Simulation shows UTB SOI has excellent Ioff and S if Tsi < Lg/4. Lg = 20 nm, Vds = 1 V, lightly doped body [71].

2.6.4. Full depletion in silicon thin-films

It is important to introduce the concept of full depletion of thin-films to better understand the advantages of the FinFET [22]. Figure 2.23 illustrates the band diagram of four different possible devices defined by the thickness of the silicon layer and the gate bias. In Figure 2.23 the following devices have been considered:

- Bulk MOSFET
- Thick-film on SOI
- Horizontal thin-film on SOI
- Vertical thin-film on SOI

Si-bulk is considered with the SOI condition. The only difference may rise at the junction level that, in the case of SOI, they are completely separated from the bulk, while for the local SOI are still connected. For a standard bulk device (Figure 2.23a), the depletion zone (the region where the charge carriers have been repulsed away from the gate electric field) extends from the Si-Oxide interface to a maximum depletion width given by:

$$X_{dmax} = \sqrt{\frac{4\ \varepsilon_{Si}\,\Phi_F}{q\,N_A}} \tag{2.37}$$

where ε_{Si} is the silicon dielectric constant, φ_F is the Fermi potential, N_A is the channel doping concentration, and q is the elementary charge. The Fermi potential Φ_F for p-type silicon is given by:

$$\Phi_F = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{2.38}$$

where k is the Boltzmann constant, T the temperature, and n_i the intrinsic carrier concentration of silicon. The potential outside the depletion regions becomes linear in the bulk, known as body, characterized by a neutral space charge distribution.

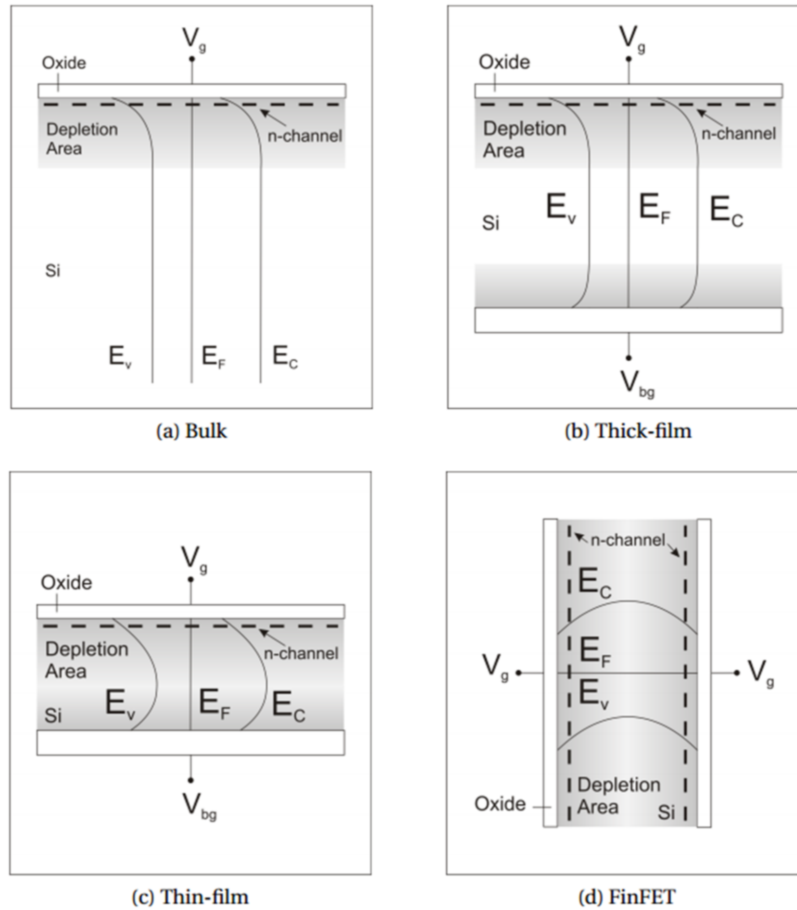

Figure 2.23 Distinction between bulk, thick- and thin-film: band diagram with depletion regions in a bulk (a), a thick-film (b), a thin-film with back-gate (c) and a FinFET (d) [72].

For a thick film, the back-gate is biased to create another depleted (or accumulated) region. The silicon thickness becomes comparable to X_{dmax}, but the depleted regions are still divided by a portion of neutral silicon (Figure 2.23b). Such a condition is defined as partial depletion (PD). When the two depleted regions start to interact, i.e. x_{dmax} has become larger than the silicon film, the condition of full depletion (FD) applies and the device is referred to as thin-film (Figure 2.23c). If the structure is rotated by 90° and a common gate controls the conduction on the vertical channels, the potential distribution is directly symmetric, which is the case for FinFETs (Figure 2.23d). Moreover, for vertical structures the use of a back-gate is less needed, since almost the whole surface of the vertical structure is controlled by the front gate. As for bulk MOSFET (Figure 2.23), the potential distribution $\Phi(x,y,z)$ inside the FinFET channel can be obtained by solving the Poisson's equation using the depletion approximation:

$$\frac{d^2\,\Phi\,(x,y,z)}{dx^2} + \frac{d^2\,\Phi\,(x,y,z)}{dy^2} + \frac{d^2\,\Phi\,(x,y,z)}{dz^2} = \frac{q\,N_a}{\varepsilon_{Si}} \tag{2.39}$$

For a double-gate device, $\frac{d\,\Phi}{dz} = 0$ [2], and the Poisson's equation becomes:

$$\frac{d^2\,\Phi\,(x,y,z)}{dx^2} + \frac{d^2\,\Phi\,(x,y,z)}{dy^2} = \frac{q\,N_a}{\varepsilon_{Si}} \tag{2.40}$$

An approximate solution of Eq. 2.35 can be found by assuming a parabolic potential distribution in the y-direction [73]. However, a more detailed solution should take into account the top gate of a FinFET as reported in [74], where a complex 3D analytical solution of the Poisson's equation is proposed, comparing the results to numerical solutions. It is also worth mentioning how the threshold voltage V_{th} of a FinFET can be modified from the MOSFET equivalent one. The V_{th} is usually defined as the voltage at which strong inversion occurs. For a MOSFET it is expressed by [75]:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{q\,N_A\,x_{dmax}}{C_{ox}} \tag{2.41}$$

where V_{FB} is the flat band voltage equal to the work function difference between metal and silicon, φ_M - φ_{Si}, and C_{ox} is the gate capacitance per unit area (surface and oxide charges are neglected). The term qN_Ax_{dmax} represents the depletion charge Q_D.
In a fully depleted FinFET, Q_D is constant and it becomes [2]:

$$Q_{D_{Fin}} = q\frac{1}{2}\,T_{Fin}\,N_A \tag{2.42}$$

The above expression is valid as long as the thickness of the inversion layer is small with respect to the silicon film thickness. Also, for ultra-thin devices ($T_{Fin} \approx 10$ nm) more complex interactions should be taken into account, especially volume inversion [76].
The final gate and threshold voltage can then be expressed as:

$$V_g = \Phi_S + V_{FB} + \frac{Q_{D_{Fin}}}{C_{ox}} \tag{2.43}$$

and, at threshold,

$$V_{th} = 2\Phi_f + V_{FB} + \frac{Q_{D_{Fin}}}{C_{ox}} \tag{2.44}$$

where Φ_S is the surface potential equal to $2\Phi_f$ in strong inversion.

3. High-k dielectrics

Increasing power consumption and degrading device performance are observed when SiO_2 is used as gate insulator [77]. Therefore, the high-κ dielectric materials are considered as promising solution to improve the gate control on the channel region and the electrical performance [78]. In this work, another important element of the presented study ZrO_2 is introduced. Such an oxide is part of the group of oxides called "high-k". First, the role of high-k dielectrics in microelectronics and their fabrication challenges are described. Later, the influence of different oxides on electrical characteristics is also discussed. Despite the fact that it is not common to talk about high-k dielectrics for all applications, it is not a coincidence that ZrO_2 represents one of the best option for both fields. Commonly, the term high-k describes a bulk property [72].

3.1. Advantages of high-k oxides in electronics

The increase of the calculating capacity of electronic devices has been realized with the continuous miniaturization of MOS transistors. The transistor scaling process has not only increased the package density of integrated circuits, but it also improved the circuit speed. According to Moore's law [79], the number of transistors within integrated circuits doubles approximately every two years and the Semiconductor Roadmap provides the factor scaling of each design parameter. How much the scaling can continue over time is not defined. However, the limits were envisaged to be in lithography, but it turns out that materials have also strict constraints to be taken into account. In the scaling process, the thickness of SiO_2, which has been used for more than 40 years, has shrunk to as little as five atomic layers (1.2 nm). These very thin layers brought along many disadvantages such as:

- Too high leakage current through direct tunnelling, resulting in energy waste and a build-up of heat;
- Reduction of the breakdown voltage and the oxide reliability;
- Control growth and uniformity of such small thicknesses.

As a solution, new gate oxides with physically thicker layer but higher permittivity started to replace SiO_2:

$$C_{ox} = \frac{\varepsilon_0 k A}{t_{ox}} \tag{2.45}$$

where ε_0 is the vacuum permittivity, k is the relative permittivity, A is the capacitance area, and t_{ox} is the oxide thickness. An oxide with a higher dielectric constant allows the use of a

physically thicker layer but with the same capacitance per unit area as that required by SiO_2. This is called the equivalent oxide thickness (EOT). When dealing with high-κ dielectrics it is more instructive to interpret EOT as the thickness of SiO_2 that would be required to achieve the same areal capacitance as the high- κ material in consideration. The thickness of gate oxide should be decreased to maintain proper electric field according to the device scaling down. ITRS referred that sub 1 nm effective oxide thickness gate stacks are required at the roadmap in 2009 [80]. When the SiO_2 reaches thickness below 1 nm, it causes the gate leakage problem due to the quantum mechanical tunneling **[77]**. Thus, as gate insulator, SiO_2 should be replaced with higher permittivity (high-k) dielectric material. With high-k dielectric layer, effective oxide thickness can be expressed as following:

$$EOT = \varepsilon_{SiO_2}\left(\frac{t_{SiO_2}}{\varepsilon_{SiO_2}} + \frac{t_{High-k}}{\varepsilon_{High-k}}\right) \quad (2.46)$$

$$EOT = k_{SiO_2}\frac{t_{High-k}}{k_{High-k}} = 3.9\ \frac{t_{High-k}}{k_{High-k}} \quad (2.47)$$

where t_{High-k} is the physical thickness of high-k dielectric layer, k_{SiO2} and k_{High-k} are the dielectric constant of SiO_2 and high-k material, respectively. For instance, with a dielectric constant of 20 and 5 nm physical thickness, effective oxide thickness of 1 nm SiO_2 can be replaced (Figure 2.24). The capacity of the dielectric layer is the same for all three structures. According to quantum mechanics, the tunneling probability increases exponentially as a function of the barrier (gate dielectric layer in this case) thickness [81]. Thus, increased dielectric thickness can avoid tunneling induced gate leakage.

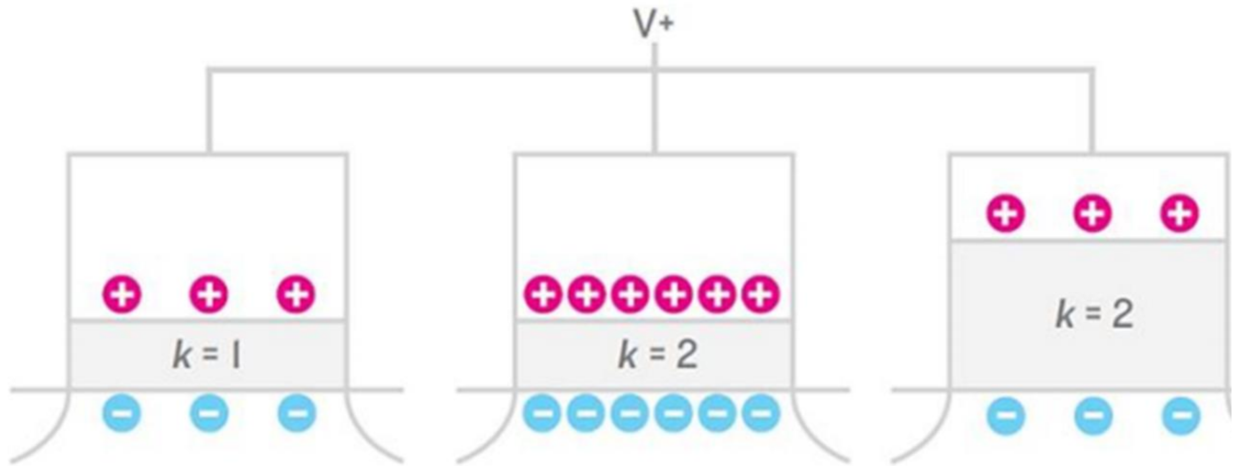

Figure 2.24 Schematics of high-*k* gate dielectric. If one gate oxide has twice k of another, a given voltage will draw twice charge into the transistor channel. Or, the same amount of charge will accumulate, if the higher-*k* dielectric is made twice as thick [77].

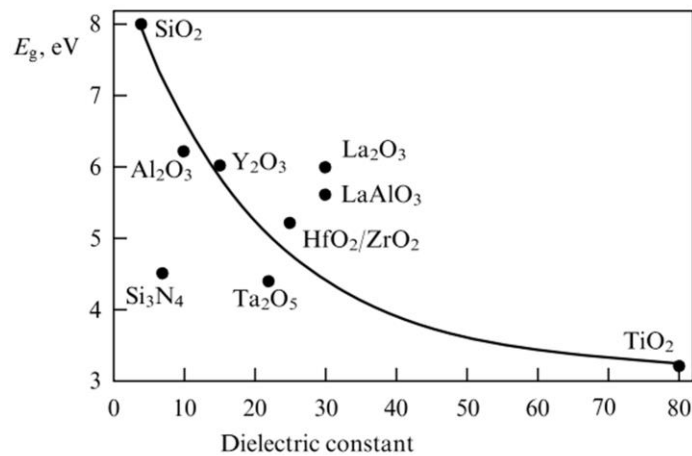

Figure 2.25 Band gap width vs static dielectric constant for a dielectric.

The simultaneous requirements of a high dielectric constant and a wide band gap contradict each other. As seen from Figure 2.25, the higher the dielectric constant, the narrower the band gap of the dielectric. With this condition, the spectrum of acceptable alternative dielectrics is limited to those with not too large dielectric constant. Materials with extremely high dielectric constant, for example, barium titante ($BaTiO_3$, ε~1000), have too small band gaps.

Potential energy barrier for electrons and holes at the dielectric-contact interface respectively determine the electron and hole injection currents. For a dielectric to be able to

block these currents, the potential barriers should exceed 1 eV. Figure 2.26 presents a schematic for electron and hole potential barriers at the interface between silicon and known high-k dielectrics.

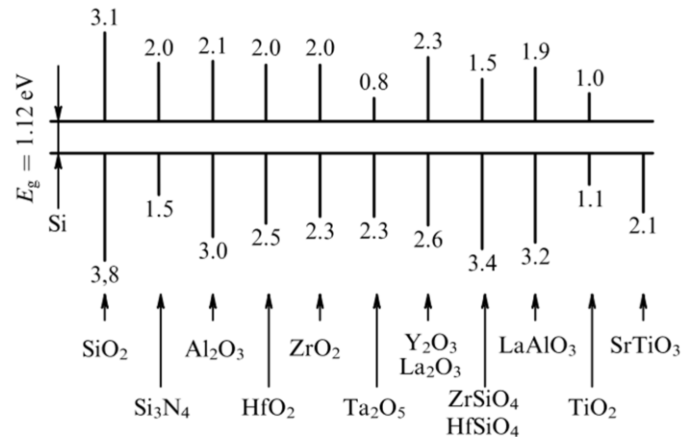

Figure 2.26 Energy diagram of the interface between silicon and dielectrics used in silicon devices, with the potential barriers for electrons and holes indicated (in electron volts).

Thermal oxide SiO_2 is also used as an insulator in memory capacitors used in static and dynamic random-access memory (RAM) **[82],** the capacity of RAM is increased by decreasing the area of storage condensed cells. For this, it is necessary to decrease the thickness of the dielectric layer in order that the electric capacity of the storage condensers not decreases. But a small oxide thickness increases the leakage current of the storage condenser, leading to the spread of the charge accumulated on the condenser plates. The leakage current of a RAM storage capacitor should not exceed 10^{-7} Acm^{-2}. An alternative solution to RAM scaling is to use a high-permittivity dielectric. Hence, increasing the information capacity of RAM requires using high-k dielectrics. At present, RAM capacitors use silicon nitride Si_3N_4 (ε=7.0) instead of SiO_2. The nitride and oxynitride of silicon are often called middle-k dielectrics. At present, Al_2O_3 (ε=10), Ta_2O_5 (ε=22); ZrO_2 (ε=25); HfO_2 (ε=25); and TiO_2 ($\varepsilon\approx$80) are considered promising candidates for RAM isolators.

However**,** such a replacement entails many difficulties and loss of many advantages. Indeed, the SiO_2, except when it becomes too thin, is an excellent material, with few electronic defects, excellent interface, high thermal stability and high band offset with Si. All these properties are physically and chemically connected with the low permittivity and, moving towards a higher dielectric constant, it involves losing such privileges. Moreover, the choice of a high-k oxide should take into account [83, 84]:

- Enough high dielectric constant to be used for a reasonable number of years;
- Large band offset with Si (E_G is inversely proportional to ε);
- Thermodynamic and kinetic stability;
- No reaction with Si and the metal gate;
- Good interface with Si, low lattice mismatch and similar thermal expansion coefficient;
- Few electrically active defects in its bulk;
- Negligible CV hysteresis.

The static dielectric constant and the band gap of some interesting high-k dielectrics are reported in Tab. 2.2 [85]. Considering the constraints listed above, HfO_2, ZrO_2 and La_2O_3 are the most promising candidates. Al_2O_3 and Si_3N_4 provide, in fact, a too low k-value to be implemented for several years, while TiO_2 and Ta_2O_5 have a too small energy band offset with Si. La_2O_3 has a higher k-value and band offset than HfO_2, but it has been found to be highly hygroscopic, meaning that it attracts and holds water molecules from the surrounding environment. HfO_2 and ZrO_2 are very similar in their electronic structure. Zr and Hf have both 8 oxygen neighbours and each oxygen has 4 Zr/Hf neighbours. All the parameters usually used to describe an oxide are the result of this intrinsic electronic nature. Low-k oxides, as SiO_2, are in fact characterized by a prevalence of covalent bonding with a low coordination number. On the other hand, high-k are characterized by ionic bonding with high coordination number [86]. Such a difference is not only the origin of the different bulk permittivity but it has also a large impact on the concentration of defects. The SiO_2 network, in fact, is much more able to relax, to rebound dangling bonds and remove defects, providing an excellent interface with Si. Finally, the analysis of the thermodynamic stability has revealed that ZrO_2 is actually unstable and reacts with Si and Poly-Si [87], leaving HfO_2 as the preferred high-k oxide.

Table 2.2 High-k dielectrics

Oxide	k	Gap [eV]	CB offset [eV][1]
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8
Ta_2O_5	22	4.4	0.35
ZrO_2	25	5.8	1.5

HfO_2	25	5.8	1.4
La_2O_3	30	6	2.3
TiO_2	80	3.5	0

4. Quantum Effects in FinFETs

Quantum effects play a vital role in determining the transistor characteristics of FinFET devices. In FinFET devices, the transport of the charge carriers occurs in a silicon film of a thickness in the order of a few nanometers. This nanometric film is surrounded by an isolation layer of oxide, i.e., a high potential barrier. In this study, the basic tools involved in the Atlas simulation of the quantum effect in FinFETs are provided. A comparison between the Bohm Quantum Potential (BQP) model and classical model in the simulation is also given considering their accuracy and computational efficiency. This results in significant quantum-mechanical effects (QMEs), which cannot be ignored in the device modeling and simulation. In fact, these QMEs can be grouped into three categories: (1) Quantum confinement across the transistor channel, (2) quantum-mechanical tunneling across the gate oxide, and (3) quantum transport of the charge carriers along the channel. These effects are briefly reviewed hereinafter [88].

4.1 Quantum Confinement

FinFET devices with very thin fin thickness exhibit QM confinement of the charge carriers across the channel [89]. Figure 2.27a shows a vertical cross section, and Figure 2.27b shows a horizontal cross section of a FinFET device. The origin of these confined charge carriers are from both structural [90] and electrical confinement [91]. The confinement to a thin semiconductor layer leads to a dramatic change in the device behavior. The energy levels available for motion in the y- and z-direction are quantized with a continuum for motion in the x-direction. This quantization is accompanied with the presence of the modes (or subbands), each mode with a certain band energy distribution along the channel and a certain charge carriers probability distribution across the channel [92]. The separation between these modes in energy as well as the energy of the lowest order mode becomes larger for smaller values of T_{Si} and H_{Si} and for larger gate bias voltage. Therefore, the threshold voltage can be controlled using T_{Si} and, thus, a lightly doped or intrinsic channel can be used. In many cases, H_{Si} is made much larger than T_{Si} in order to have a sufficient current flowing along the channel, such that the confinement effect can be considered in one direction only [88].

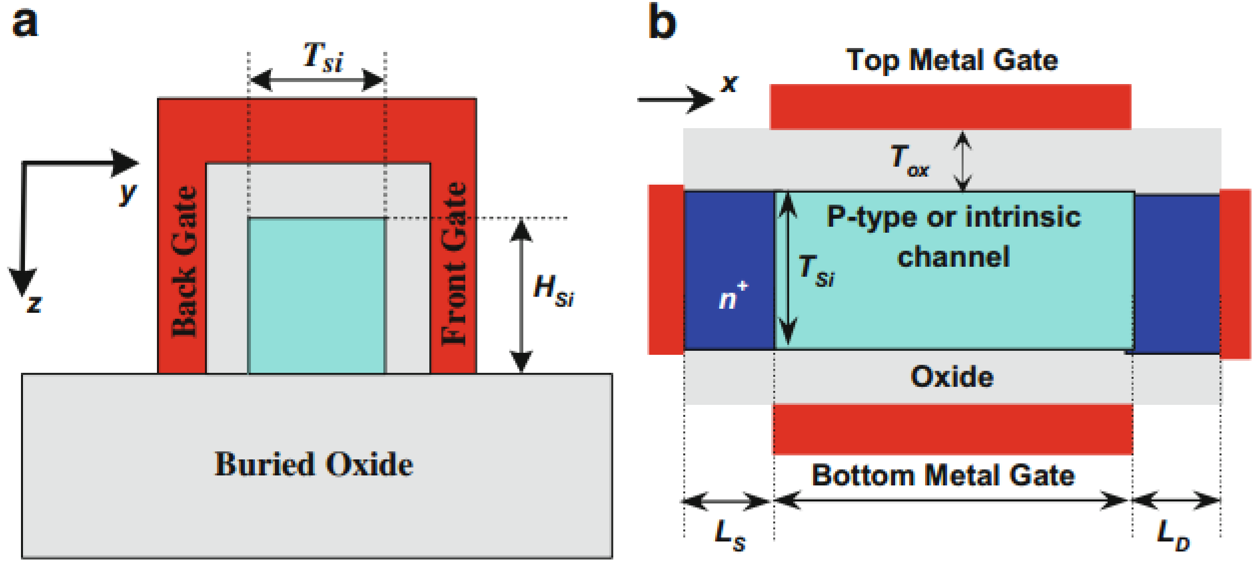

Figure 2.27 FinFET structure: (a) vertical cross section and (b) horizontal cross section [88].

The threshold voltage of a FinFET can be defined as that voltage (gate) which would be able to invert all the channels within the Fin structure simultaneously. The QM threshold voltage ($V_{th,QM}$) of the DG FinFET device structure is [93]:

$$V_{th,QM} = V_{fb} + \psi_{s(inv)} - \frac{Q_b}{2C_{ox}} + \Delta V_{th,QM} \tag{2.48}$$

where $\psi_{s(inv)}$ is the surface potential at threshold, and $\Delta V_{th,QM}$ is the threshold voltage change due to QME's, which can be approximated as a function of the ratio of the carrier effective mass in the direction of confinement to the free electron mass and silicon film thickness which is given as [94]:

$$\Delta V_{th,QM} \cong \frac{SS}{(KT/q)\ln(10)} + \frac{0.3763}{(m_x/m_0 q)T_{fin}^2} \tag{2.49}$$

where SS is the subthreshold slope and m_x/m_o is the ratio of the carrier effective mass in the direction of confinement to the free electron mass.

The bulk charge Q_b is given as:

$$Q_b = -qN_aT_{fin} \tag{2.50}$$

when considering the quantum-mechanical confinement of inversion-layer carriers, $V_{th,QM}$ of (4.43) should be augmented with $\Delta V_{th,QM}$. The surface potential at threshold is given by:

$$\psi_{s(inv)} = 2\ \psi_b \tag{2.51}$$

$$\psi_b = \frac{KT}{q}\ln\left(\frac{N_a}{N_i}\right) \tag{2.52}$$

Substituting the value of ψ_b from (2.47) into (2.46), we obtained:

$$\psi_{s(inv)} = 2\left(\frac{KT}{q}ln\left(\frac{N_a}{N_i}\right)\right) \tag{2.53}$$

Substituting the value of Q_b from (2.45), $\psi_{s(inv)}$ from (2.48) and $\Delta_{Vth,QM}$ from (2.44) into threshold expression (2.43), the final expression for the threshold voltage with QM corrections is obtained as:

$$V_{th,QM} = V_{FB} + 2\left(\frac{KT}{q}ln\left(\frac{N_a}{N_i}\right)\right) - \frac{(-qN_aT_{fin})}{2C_{ox}} + \frac{SS}{\left(\frac{KT}{q}\right)\ln(10)}\ x\ \frac{0.3763}{(m_x/m_0)T_{fin}^2} \tag{2.54}$$

To obtain the quantum electrical characteristics of a considered FinFET device structure, the BQPohm Quantum Potential model is used in Atlas 3D simulations, which is Bohm’s interpretation of quantum mechanics. The quantum confinement is correctly predicted by the BQP model.

4.1.1 Bohm Quantum Potential (BQP)

The BQP model is an expansion of the Wigner equation and calculates the effects of quantum confinement on the electrons and holes concentration and C-V curves [95]. This model was developed for SILVACO by the University of Pisa and has been implemented into ATLAS with the collaboration of the University of Pisa. This is an alternative to the Density Gradient method and can be applied to a similar range of problems. There are two advantages to using BQP over the density gradient method. First, it has better convergence properties in many situations. Second, possibility to calibrate it against results from the Schrödinger-Poisson equation under conditions of negligible current flow. The Bohm interpretation is causal but not local and it is non-relativistic.

The Bohm interpretation is based on these principles:

- Every particle travels in a definite path
- We do not know what that path is

- The state of N particles is affected by a 3N dimensional field, which guides the motion of the particles

  De Broglie called this the pilot wave; Bohm called it the ψ-field. This field has a piloting influence on the motion of the particles. The quantum potential is derived from the ψ-field.

- This 3N dimensional field satisfies the Schrödinger equation

  Mathematically, the field corresponds to the wavefunction of conventional quantum mechanics, and evolves according to the Schrödinger equation. The positions of the particles do not affect the wave function.

- Each particle's momentum p is $\frac{\partial S(x,t)}{\partial x}$
- The particles form a statistical ensemble, with probability density $\rho(x, t) = |\psi(x,t)|^2$

Some of Bohm's insights are based on a reformulation of the Schrödinger equation; instead of using the wave function $\psi(x,t)$, he defines the wave function as

$$\psi(x,t) = R(x,t)e^{\frac{iS(x,t)}{\hbar}} \tag{2.55}$$

and solves it for the (real) magnitude function R(x, t) and (real) phase function S(x, t).

The Schrödinger equation for one particle of mass m is:

$$i\hbar\frac{\partial\psi(x,t)}{\partial t} = -\frac{\hbar^2}{2m}\frac{\partial^2\psi(x,t)}{\partial x^2} + V(x)\,\psi(x,t) \tag{2.56}$$

where the wave function $\psi(x,t)$ is a complex function of the spatial coordinate x and time t. It can then be split into two coupled equations by expressing it in terms of R and S:

$$\frac{\partial R(x,t)}{\partial t} = -\frac{1}{2m}\left[R(x,t)\frac{\partial^2 S(x,t)}{\partial x^2} + 2\frac{\partial\psi(x,t)}{\partial x}\ \frac{\partial S(x,t)}{\partial x}\right] \tag{2.57}$$

$$\frac{\partial S(x,t)}{\partial t} = -\left[V + \frac{1}{2m}\left(\frac{\partial S(x,t)}{\partial x}\right)^2 - \frac{\hbar^2}{2m\,R(x,t)}\ \frac{\partial^2 R(x,t)}{\partial x^2}\right] \tag{2.58}$$

The probability density ρ(x, t) is a real function defined as the magnitude of the wave function:

$$\rho(x, t) = |\psi(x,t)|^2 = R^2(x,t) \tag{2.59}$$

thus

$$\psi(x,t) = \sqrt{\rho(x,t)e^{\frac{iS(x,t)}{\hbar}}} \tag{2.60}$$

Therefore we can substitute ρ(x, t) for $R^2(x,t)$ and get:

$$-\frac{\partial\rho(x,t)}{\partial t} = -\frac{1}{2m}\left[\rho(x,t)\frac{1}{m}\frac{\partial S(x,t)}{\partial x}\right] \tag{2.61}$$

$$-\frac{\partial S(x,t)}{\partial t} = V(x) + Q(x,t) + \frac{1}{2m}\left(\frac{\partial S(x,t)}{\partial x}\right)^2 \tag{2.62}$$

Where

$$Q(x,t) = -\frac{\hbar^2}{2m\,R(x,t)}\frac{\partial^2 R(x,t)}{\partial x^2} = -\frac{\hbar^2}{2m\sqrt{\rho(x,t)}}\frac{\partial^2 \sqrt{\rho(x,t)}}{\partial x^2} \tag{2.63}$$

Bohm called the function $Q(x,t)$ the quantum potential.

SILVACO has already included in its device simulator ATLAS, a Schrödinger-Poisson solver and Density-Gradient model. The Schrödinger-Poisson (SP) solver is the most accurate approach to calculate the quantum confinement in semiconductor but it cannot predict the currents flowing in the device. To overcome this limitation, ATLAS provides a Density Gradient (DG) model [1]. It allows the user to predict both the quantum confinement and the drift-diffusion currents along with the Fermi-Dirac statistics for a 2D structure.

However this model exhibits poor convergence in 3D and with the hydrodynamic transport. Therefore, in collaboration with the University of Pisa, SILVACO has introduced in ATLAS, a new approach called Effective Bohm Quantum Potential (BQP) model. This model exhibits many advantages. It includes two fitting parameters which ensure a good calibration for silicon or non-silicon materials, planar or non-planar devices. It is numerically stable and robust, and independent of the transport models used. Therefore, it has been successfully implemented and tested in ATLAS. The BQP model does not depend on the transport model (drift-diffusion or hydrodynamic); Fermi-Dirac statistics can be straightforwardly included; it provides two parameters for calibration, whereas the Density Gradient has only one fitting parameter; finally, it exhibits very stable convergence properties.

To solve the non-linear BQP equation along with a set of semi-classical equations is as follows. After an initial semi-classical solution has been obtained, the BQP equation is solved on its own Gummel iteration to give Q at every node in the device. The semi-classical potential is modified by the value of Q at every node and the set of semi-classical equations is then solved to convergence as usual (using a Newton or Block iterative scheme). Then, the BQP equation is solved to convergence again and the process is repeated until self-consistency is achieved between the solution of the BQP equation and the set of semi-classical equations. The set of semi-classical equations solved can be any of the combinations usually permitted by ATLAS. To use the BQP model for electrons (or holes), we need to specify BQP.N (BQP.P) in the MODELS statement [96].

The Bohm Quantum Potential (BQP) method can also be used for the Energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential the same way as for the continuity equations. The continuity equations for electrons and holes are defined by equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\, div\,\overrightarrow{J_n} + G_n - R_n \tag{2.64}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\, div\,\overrightarrow{J_p} + G_p - R_p \tag{2.65}$$

where n and p are the electron and hole concentration, and are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on an electron.

4.2 Quantum-Mechanical Tunneling

Two QM tunneling effects are likely generated in very thin device such as FinFET, tunneling through the gate oxide and source-to-drain tunneling along the transistor channel. Gate oxide tunneling is unavoidable for oxide thickness smaller than 7 nm [97]. For the FinFETs, the oxide thickness is typically less than 2 nm, and the direct tunneling mechanism dominates the other mechanisms [98]. For this reason, high-k dielectric material is used instead of silicon oxide such that their physical thickness can be larger while their effective thickness, corresponding to the oxide capacitance, is the same [98]. The gate leakage current can be accounted for within the quantum transport simulation in the real-space representation. The source-to-drain tunneling current becomes important for channel lengths below 5 nm [99]. Indeed, this mechanism is automatically accounted for within the calculation of the source to drain current without paying any extra attention.

4.3 Ballistic Transport and Quantum Interference

The phase breaking length is defined as the distance over which the electron wave's phase is destroyed by some process. It was estimated to be in the range of 50 nm for silicon [91]. The phase breaking process arises from the interaction of the electron with phonons (lattice vibrations), photons (electromagnetic vibrations), or other electrons. For macroscopic devices, phase randomizing scattering dominates, and electrons wave's phase is randomized by collisions and lose their phase during the transport process. Therefore, quantum interference effects can be neglected in macroscopic devices, and a semiclassical approach based on Boltzmann transport equation can be used to describe the transport [100]. In the nanometric devices the dimensions of which are much larger than the atoms but smaller than scattering events, the electrons may transport ballistically from one side of the device to the other side without scattering. In this case, the phase of the electrons wave nature plays an

important role in the transport process because electrons can interfere instructively or destructively. It was shown that carrier density oscillations can be found near the channel barrier edges especially at low temperature [97]. At room temperature or higher, the interference effect is washed out by the statistics. Ballistic transport and carrier interference are intrinsically accounted for in the transport simulation.

CHAPTER III: FABRICATION AND SIMULATION

This chapter presents different methods which have been reported for the virtually fabrication of silicon fin field-effect transistor (FinFET) using Technology Computer Aided Design (TCAD) tools. TCAD is a high-level of electronic design automation that models semiconductor fabrication and semiconductor device operation. The modelling of the fabrication is termed Process TCAD, while the modelling of the device operation is termed Device TCAD. Any semiconductor device is represented by a structure which electrical and physical properties are discretized onto a mesh of nodes. The two/three-dimensional device structure may be the output of the process simulator or can be supplied from an input file containing the mesh information, types of materials, doping profiles in specific regions, names of the terminals, and properly defined boundary conditions with applied external electrical, optical, mechanical, magnetic, and thermal fields. In addition, included are the modelling of process steps (such as diffusion and ion implantation), and modelling of the behaviour of the electrical devices based on fundamental physics, such as the doping profiles of the devices. This technology may also include the extraction of compact model parameters (such as the well-known SPICE transistor models), which try to capture the electrical behaviour of such devices but, generally, don't derive them from the underlying physics. In this section, there would be shown overall process flow for FinFET include fabrication using ATHENA, the technique for existence of different materials in this software and simulation in ATLAS. Regarding to this part, it is easy to understand how to improve sample FinFET to get optimize performance. In the development of advanced FET, feedback between device fabrication and characterization is essential for the device optimization. Therefore, accurate parameter extraction is very important in the advanced devices.

3.1 Silvaco's TCAD Software

Silvaco, Inc. is a leading EDA provider of software tools used for device development process and for analog/mixed-signal, power IC, and memory design. Silvaco delivers a full TCAD-to-Signoff flow for vertical markets including: displays, power electronics, optical devices, radiation & soft error reliability and advanced CMOS process and IP development. For over 30 years, Silvaco has enabled its customers to bring superior products to market with reduced cost and in the shortest time. The company is headquartered in Santa Clara, California, and has a global presence with offices located in North America, Europe, Japan and Asia [102].

Semiconductor process simulation is the modeling of the fabrication of semiconductor devices such as transistors. It is a branch of electronic design automation, and part of a sub-field known as technology CAD, or TCAD [102].

Technology files and design rules are essential building blocks of the integrated circuit design process. Their accuracy and robustness over process technology, its variability and the operating conditions of the IC — environmental, parasitic interactions and testing, including adverse conditions such as electro-static discharge — are critical in determining performance, yield and reliability. Development of these technology and design rule files involves an iterative process that crosses boundaries of technology and device development, product design and quality assurance. Modeling and simulation play a critical role in supporting many aspects of this evolution process. The goals of TCAD start from the physical description of integrated circuit devices, considering both the physical configuration and the related device properties, and build the links between the broad range of physics and electrical behavior models that support circuit design. Physics-based modeling of devices, in distributed and lumped forms, is an essential part of the IC process development. It attends to quantify the key parameters that support the circuit design and the statistical metrology [102].

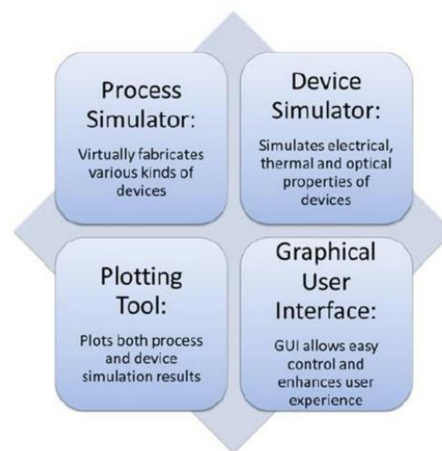

Figure 3.1 A typical TCAD software suite [4].

This software has its own license and it works under many operative systems such as Macros, Window, and LINUX. Silvaco takes step further by generate important software in analysis semiconductor in future circuit level, which is ECAD. The software package use in this project also calls Virtual Wafer Fabricate (VWF) that includes several different programs as shown in Figure 3.2.

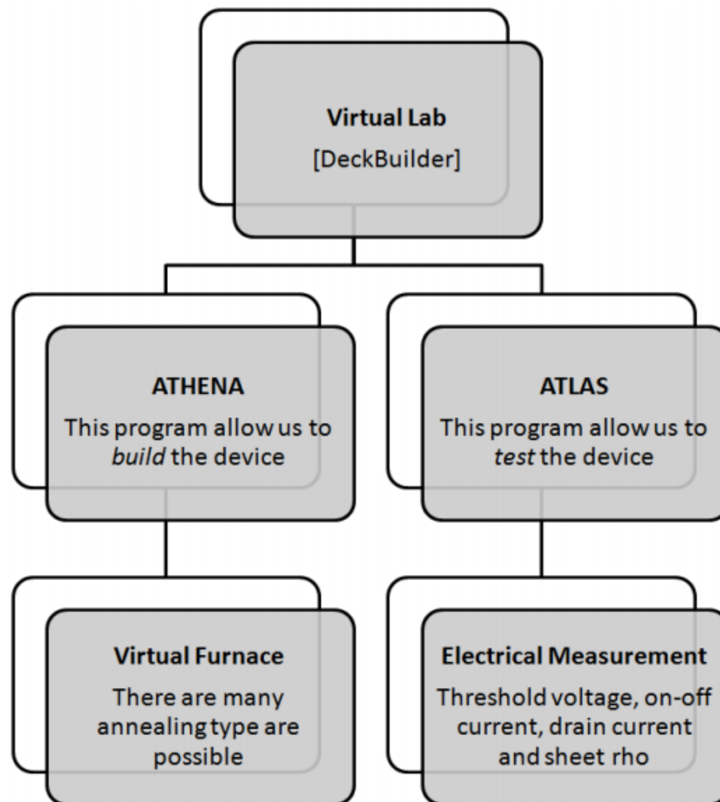

Figure 3.2 Silvaco's Virtual Wafer Fabrication environment [4].

TCAD simulators can model the electrical, optical, thermal, and sometimes even the mechanical properties of devices. They can be used in standalone mode by defining the device structure or used in conjunction with a process simulator. These tools allow the user to work on band structure engineering, quantum confinement, and other optimizations that would be difficult to accomplish using experimental results alone. Most device simulators are based on 2D/3D finite element analysis of electrical, thermal, and optical properties of material and silicon semiconductor devices [4]. In general, the device TCAD includes a suite of physical models describing carrier transport in materials. Device models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and computationally challenging models such as the energy balance, which solves some higher moment simplification of the Boltzmann transport equation (BTE). In addition, the complex physics of today's nanoscale devices mandates the use of Monte Carlo (MC) codes, which stochastically solves BTE, and the use of Schrödinger solvers that account for quantum mechanical effect (QME) effects in field-effect transistor (FET) devices. The choice of the appropriate model depends on the problem and on the level of detail required. Despite the significant advances of both numerical modeling and physics, continuous development is

required to meet the increasingly challenging industry needs for device exploration, scaling, and optimization. Therefore, the ability of device CAD to accurately model today's device performance and predict tomorrow's device limitations is of utmost importance. Though the process CAD and device CAD refer to numerical simulation of different areas of computational electronics, they are synergistically linked [4].

3.1.1 ATHENA

ATHENA is a framework program that combines several smaller programs to be a complete simulation tools. This can change from one dimensional view, 1D to two dimensional view, and 2D process. The focus of this program is to do simulation for wide range of fabrication process. This sub-VWF can easily work and provide modular and extensible platform for simulating diffusion, etching, lithography, oxidation, and silicidation of semiconductor materials. Figure 3.4 shows the input and output of ATHENA program [4].

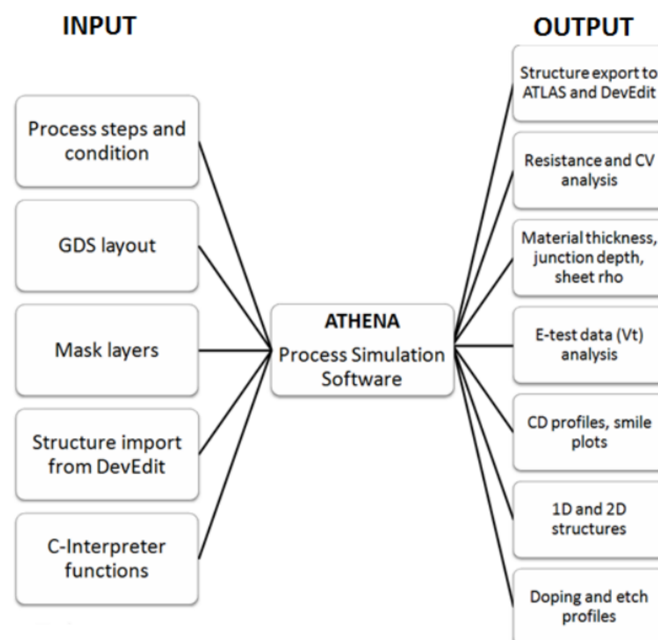

Figure 3.4 THENA inputs and output **[4]**.

3.1.2 ATLAS

ATLAS is a device simulation tool. The framework of ATLAS combines several one-, two-, and three-dimensional simulation tools into one comprehensive device simulation package. This allows for the simulation of a wide variety of modern semiconductor devices. It is a physically based predictive device simulator that predicts the electrical characteristics

associated with specified physical structures and bias conditions to provide insight within device operation and behaviour [4].

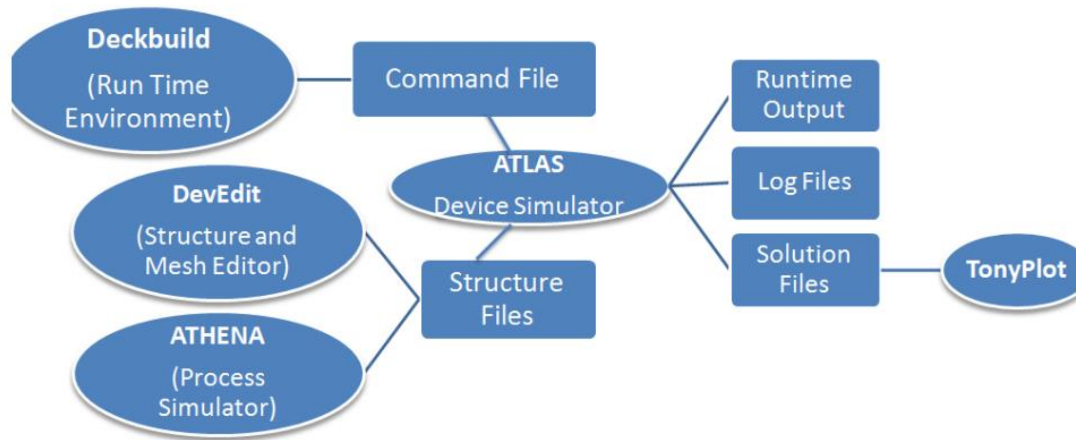

Figure 3.5 ATLAS environments [4].

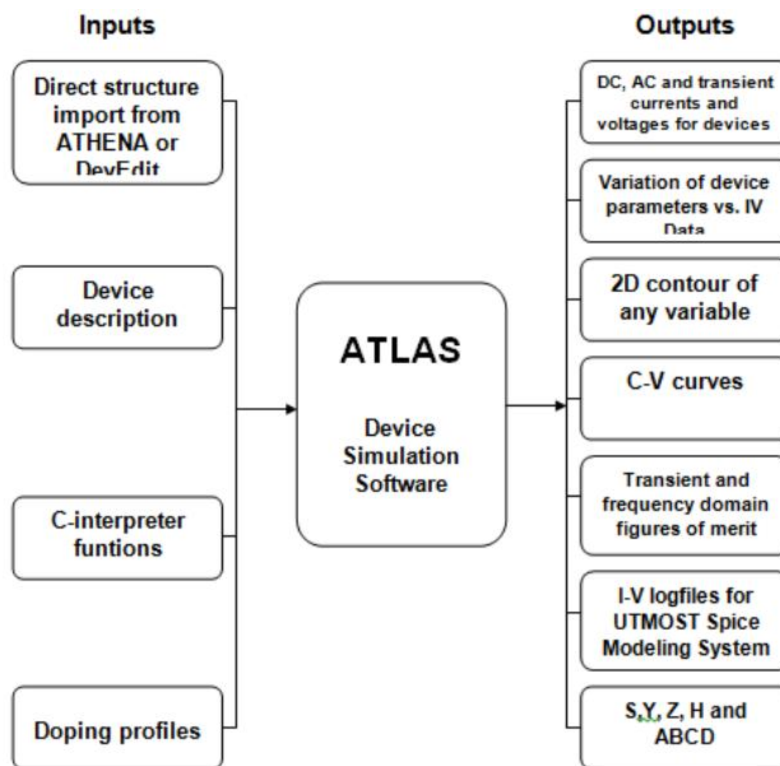

Figure 3.6 ATLAS inputs and outputs [4].

3.1.3 DECKBUILD

DeckBuild is the front-end GUI (Graphical User Interface) for Silvaco's Virtual Wafer Fab programs. This program is the framework which ties together the wide range of process and device simulation tools available, and allows them to work together seamlessly

and efficiently. DeckBuild uses pull-down menus to generate syntax for the various programs and provides basic simulation controls such as run, kill, pause, stop-at, re-start, single-step, and history initialization operations [4].

3.1.4 DEVEDIT

DEVEDIT is a program that allows for structure editing, structure specification and grid generation graphically by drawing on the screen (interactively) or in batch mode (running a script file). All of Silvaco's programs use a mesh or grid. They are used to determine the level of detailing the simulation will generate in a specific area of the device. Therefore, it allows users to cut down the simulation time by removing detailing from areas with less interest containing uniform or no reaction to change/alter simulation results. The creation of these meshes is the main function of DEVEDIT; however, it is also used for the editing and specification of two- and three-dimensional devices created with the VWF tools **[4]**. DEVEDIT can be used interactively only under a Linux operating system.

3.1.5 TONYPLOT

TonyPlot is a graphical post-processing tool for use with all TCAD Silvaco simulators and interactive tools such as DeckBuild, VWF or SPDB. TonyPlot provides comprehensive capabilities for viewing and analysing simulator output. Wide range of supported plots including 2D plots, X-Y plots, polar plots, Smith plots, cross-section, RSM plots (1D, 2D, and 3D) and statistical plots. In addition, multiple files can be loaded and overlaid in a plot for comparison. Besides that, it integrates 1D cross-section of 2D plots, rulers, probe, integrators, and other tools. Last but not least, TonyPlot enables 2D structures plots to be cut by multiple, independently controlled 1D slice [4].

3.2 Physical models

3.2.1 Mobility models

Electrons and holes are accelerated by electric fields, but lose momentum because of various scattering processes. These scattering mechanisms include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections. Since the effects of all these microscopic phenomena are lumped into the macroscopic mobility introduced by the transport equations these mobility is therefore functions of the local electric field, lattice temperature, doping concentration, and so on. Mobility modeling usually is

divided into: (i) low-field behavior, (ii) high field behavior, (iii) bulk semiconductor regions and (iv) inversion layers. The low electric field behavior has carriers almost in equilibrium with the lattice and the mobility has a characteristic low-field value that is commonly denoted by the symbol $\mu_{n0,p0}$ (the index n and p denotes electrons and holes, respectively). The value of this mobility is dependent upon phonon and impurity scattering. Both of which act to decrease the low field mobility [4].

The high electric field behavior shows that the carrier mobility declines with electric field because the carriers that gain energy can take part in a wider range of scattering processes. The mean drift velocity no longer increases linearly with increasing electric field, but rises more slowly. Eventually, the velocity doesn't increase any more with increasing field but saturates at a constant velocity. This constant velocity is commonly denoted by the symbol V_{sat} (saturation velocity). Impurity scattering is relatively insignificant for energetic carriers, and so V_{sat} mainly depends on the lattice temperature. Modeling mobility in bulk material involves:

- Characterizing μ_{n0} and μ_{p0} as a function of doping and lattice temperature;
- Characterizing V_{satas} a function of lattice temperature;
- Describing the transition between the low-field mobility and saturated velocity regions;

Modeling carrier mobility in inversion layers introduces additional complications. Carriers in inversion layers are subject to surface scattering, extreme carrier-carrier scattering, and quantum mechanical size quantization effects. These effects must be accounted for in order to perform accurate simulation of FET devices. The transverse electric field is often used as a parameter that indicates the strength of inversion layer phenomena. Therefore, in order to achieve a successful prediction of a FinFET device, it is necessary to use multiple non-conflicting mobility models simultaneously. It is also necessary to know which models are overriding others when conflicting mobility models are defined [4].

3.2.2 Shirahata's Mobility Model

The Shirahata Mobility Model is a general purpose MOS mobility model that accounts for screening effects in the inversion layer and uses improved perpendicular field dependence for thin gate oxides. The Shirahata models for electrons and holes are given by [4]:

$$\mu_n = \frac{muo_n\left(\frac{T_L}{300}\right)^{-theta_n}}{\left[1+\frac{|E_{perp}|}{E_{1,n}}\right]^{P_{1,n}}+\left[\frac{|E_{perp}|}{E_{2,n}}\right]^{P_{2,n}}} \tag{3.1}$$

$$\mu_p = \frac{muo_p \left(\frac{T_L}{300}\right)^{-theta_p}}{\left[1+\frac{|E_{perp}|}{E_{1,p}}\right]^{P_{1,p}} + \left[\frac{|E_{perp}|}{E_{2,p}}\right]^{P_{2,p}}} \quad (3.2)$$

Where E_{perp} is the perpendicular electric field strength, T_L the lattice temperature and the rest equation parameters have empirically optimized values depending on the device technology.

3.2.3 Parallel Electric Field-Dependent Mobility

As carriers are accelerated in an electric field, their velocity will begin to saturate when the electric field magnitude becomes significant. This effect has to be accounted for by a reduction of the effective mobility since the magnitude of the drift velocity is the product of the mobility and the electric field component in the direction of the current flow. The following Caughey and Thomas expression is usually used to implement a field-dependent mobility that provides a smooth transition between low-field and high field behaviour [101]:

$$\mu_n(E) = \mu_{n0} \left[\frac{1}{1+\left(\frac{\mu_{n0}E}{V_{sat,n}}\right)^{beta,n}}\right]^{\frac{1}{beta,n}} \quad (3.3)$$

$$\mu_p(E) = \mu_{p0} \left[\frac{1}{1+\left(\frac{\mu_{p0}E}{V_{sat,p}}\right)^{beta,p}}\right]^{\frac{1}{beta,p}} \quad (3.4)$$

Here, E is the parallel electric field and μ_{n0} and μ_{p0} are the low-field electrons and holes mobility, respectively.

3.2.4 Generation-Recombination

Carrier generation-recombination is the process through which the semiconductor material attempts to return to equilibrium after being disturbed from it. If a homogeneously doped semiconductor is considered with carrier concentrations n (electrons) and p (holes) with equilibrium concentrations n_0 and p_0 then at equilibrium a steady state balance exists according to [4]:

$$n_0 p_0 = n_i^2 \quad (3.5)$$

Semiconductors, however, are under continual excitation whereby n and p are disturbed from their equilibrium states: n_0 and p_0. For instance, light shining on the surface of

a p-type semiconductor causes generation of electron-hole pairs, disturbing greatly the minority carrier concentration. A net recombination results which attempts to return the semiconductor to equilibrium. The processes responsible for generation-recombination are known to fall into six main categories:

- phonon transitions
- photon transitions
- Auger transitions
- surface recombination
- impact ionization
- tunneling

3.2.5 Shockley-Read-Hall (SRH) Recombination

Phonon transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. This is essentially a two-step process, the theory of which was first derived by Shockley and Read and then by Hall. The two steps involved in SRH recombination are:

- An electron (or hole) is trapped by an energy state in the forbidden region which is introduced through defects in the crystal lattice. These defects can either be unintentionally introduced or deliberately added to the material, for example in doping the material; and
- If a hole (or an electron) moves up to the same energy state before the electron is thermally re-emitted into the conduction band, then it recombines

The rate at which a carrier moves into the energy level in the forbidden gap depends on the distance of the introduced energy level from either of the band edges. Therefore, if energy is introduced close to either band edge, recombination is less likely as the electron is likely to be re-emitted to the conduction band edge rather than recombine with a hole which moves into the same energy state from the valence band. For this reason, energy levels near mid-gap are very effective for recombination.

The Shockley-Read-Hall recombination is modelled as follows [4]:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1)+\tau_n(p+p_1)} \tag{3.6}$$

with:

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{KT}\right) \tag{3.7}$$

and

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{KT}\right) \tag{3.8}$$

Where E_{trap} is the difference between the trap energy level and intrinsic Fermi level. The silicon default value is E_{trap}=0.

The lifetimes τ_n and τ_p are modeled as a product of a doping-dependent, filed-dependent, and temperature-dependent factor [4]:

$$\tau_c = \tau_{dop} \frac{f(T)}{1+g_c(F)} \tag{3.9}$$

where c=n or p.

3.2.6 Band-to Band tunneling

If a sufficiently high electric field exists within a device local band bending may be sufficient to allow electrons to tunnel from the valence band into the conduction band. An additional electron is therefore generated in the conduction band and a hole in the valence band. This generation mechanism is implemented into the right-hand side of the continuity equations. The tunneling generation rate is [4]:

$$G_{BBT} = DBB.AE^{BB.GAMMA} \exp\left(-\frac{BB.B}{E}\right) \tag{3.10}$$

Where E is the magnitude of the electric field, D is a statistical factor, B.A, BB.B, and BB.GAMMA are calculated from the first principles as follows [4]:

$$BB.A = \frac{q^2\sqrt{(2 \times MASS.TUNNEL m_0)}}{h^2\sqrt{EG300}} \tag{3.11}$$

$$BB.B = \frac{\pi^2 EG300^{\frac{3}{2}}\sqrt{\frac{MASS.TUNNEL m_0}{2}}}{qh} \tag{3.12}$$

with BB.GAMMA=2

where q is the electronic charge, his Planck's constant, E_G is the energy bandgap, m_0 is the rest mass of an electron and MASS.TUNNEL is the effective mass. The bandgap at 300K, EG300, is depends on the material.

3.3 Process Flow to Develop the Environment of Project

After understand the working procedure of Silvaco's Virtual Wafer Fab and its environment [4], this study was begun with design and fabricate by using ATHENA and then proceed to ATLAS for analysis characterization of considered n-FinFET device. The flow chart of the research methodology is shown in Figure 3.7. After data collection from ATLAS User's Manual [4] FinFET structured will be designed using example FET available in Silvaco's TCAD library. From this point, this study can understand more and modified each step to get similar FinFET structure such as in a real experiment. Start with ATHENA, the FinFET structure will be created and will be proceed to ATLAS. Normally ATHENA is used for device fabrication. Once the fabrication is complete, the structure will proceed to the device simulation. In ATLAS, the input statement is applied in sequence in order to simulate the device and extract parameters from the device structure. After the simulation, the electrical parameters of the device will be determined and investigated. Next, a comprehensive analysis and comparison study will be done. This includes the analysis on both the process and characterization of the device. The data obtain are then compared with other related data. If for some reason the result is not acceptable, then all of the steps of process, device, characterization, analysis, and extracting will be repeated for validity of the new data by improving and optimizing the transistor design.

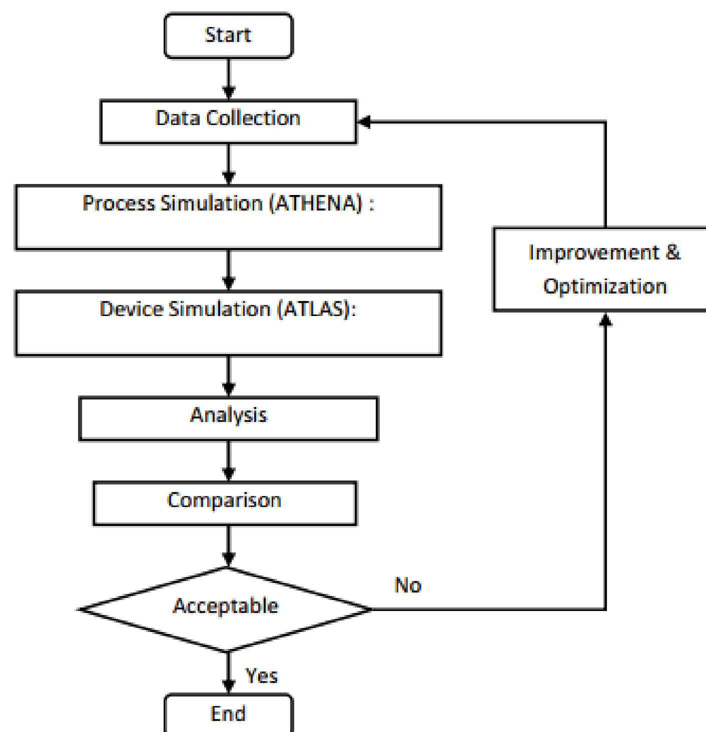

Figure 3.7 Overall process for conduct this study.

3.4 Fabrication process

Below are the fabrication process summarized into a flowchart so that the process can be follow step by step. The processes start from mesh definition and end up with the mirror structure (Mirror the structure to obtain the full symmetrical device) and labelling the electrodes.

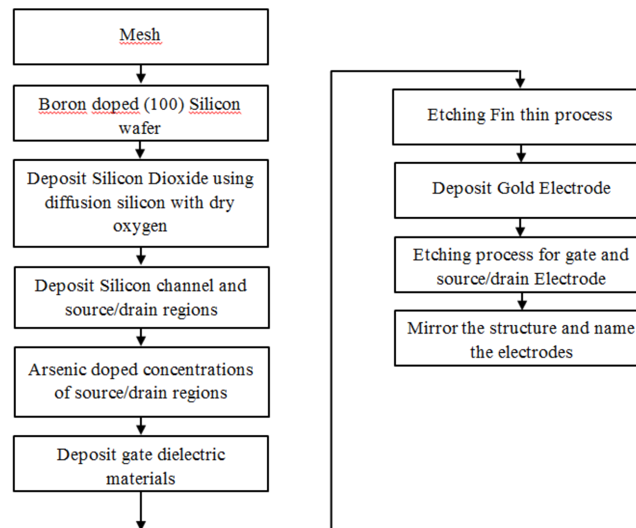

Figure 3.8 Flowchart of the 8 nm FinFET process simulation.

FinFETs have been fabricating virtually in ATHENA and then proceed analysis electrical characteristics in ATLAS. In this section, the results would be shown, discussed, and compared to modelling, real fabrication experiment, and simulation using other software or method.

Here, the series of pictures which show the output for each step in flowchart Figure 3.8. This study begins with 8 nm gate length (L_G) and 1.5 nm thick of gate dielectric material.

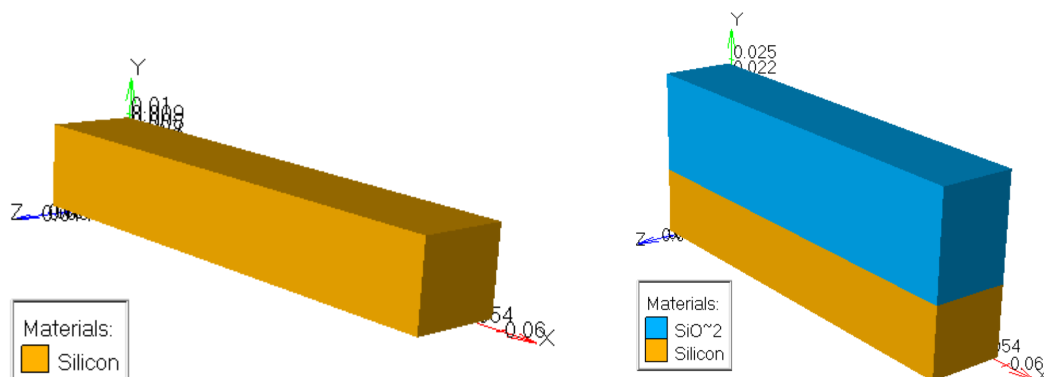

Figure 3.9 (a) P-substrate with Boron implantation (1.0e^{15} cm^{-2}) **(b)** 15 nm SiO_2 layer grown thermally (1000 $^{\circ}$C, 530 min)

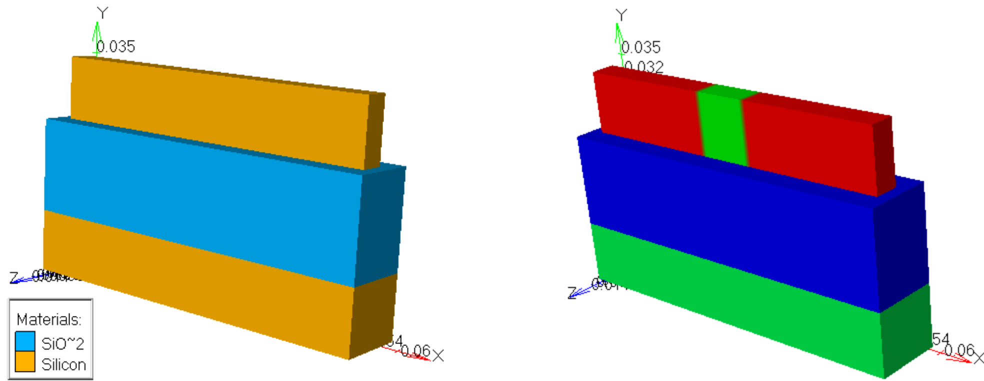

Figure 3.10 (a) thin Silicon 10 nm deposited (b) Boron implantation in the channel region ($1.0e^{15}$ cm^{-2}) and Arsenic doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3}.

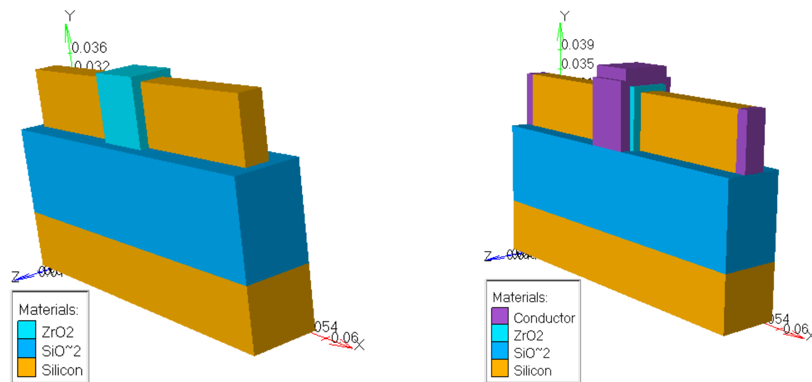

Figure 3.11 (a) Deposit ZrO_2 dielectric material around the channel region (b) Deposit Metal contact / Electrode.

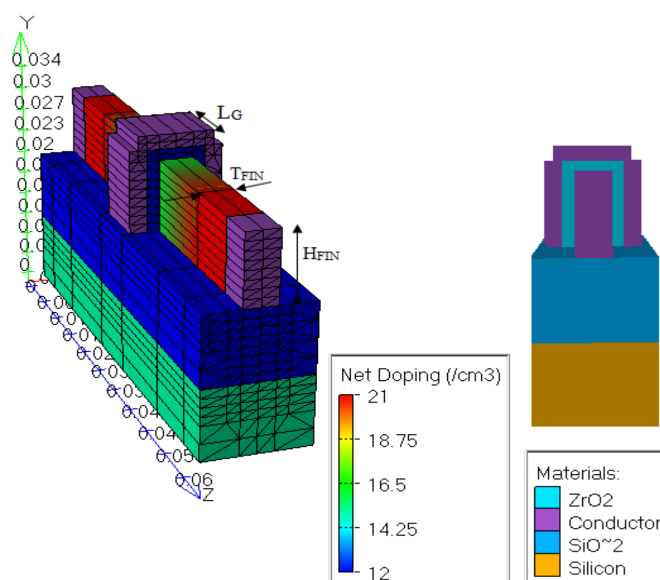

Figure 3.12 After anneals and n-FinFET successfully fabricated.

The 3D schematic view of the simulated TG FinFET structure is shown in Figure 3.12. The device dimensions, L_g, H_{FIN}, T_{FIN}, and t_{ox} are the gate length, the height of silicon fin, the thickness of silicon fin, and the thickness of gate oxide, respectively. Next, p-type silicon wafers (100) with a boron doping concentration $N_A = 10^{15}$ cm^{-3} have been thermally oxidized to a SiO_2 thickness of $t_{ox} = 15$ nm. The channel region is formed by a slightly doped volume with boron doping concentration 10^{16} cm^{-3} (P-type). The arsenic doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3}. However, arsenic has been used to produce n-type silicon to make it function as transistor and not be resistor. The thin ZrO_2 layer has been proposed to replace conventional SiO_2 gate dielectric material for good gate control of Short-Channel Effects (SCE). In TG FinFET, as depicted in Figure 3.12, the gate oxide thickness is equal in all three sides of the fin region and it has been fixed at 1.5 nm. The height of silicon fin (H_{FIN} = 10 nm) is defined as the distance between the top gate and bottom gate oxides. The thickness of silicon fin (T_{FIN} = 4 nm) is defined as the distance between front gate and back gate oxides [4]. The value of the gate work function is 4.53 eV. This structure was saved in *.str* file so ATLAS program can recall and read this file for proceed device simulation.

3.4.1 Meshing

In mathematics, the finite element method (FEM) is a numerical technique for finding approximate solutions to boundary value problems for partial differential equations. It split the whole problem domain into simpler parts, called finite elements, and the variation methods to solve the problem by minimizing the associated error function. Analogous to the idea that connecting many tiny straight lines can approximate a larger circle, FEM encompasses methods for connecting many simple element equations over many small subdomains, named finite elements, to approximate a more complex equation over a larger domain.

The subdivision of a whole domain into simpler parts has several advantages:

- Accurate representation of complex geometry
- Inclusion of dissimilar material properties
- Easy representation of the total solution
- Capture of local effects

A typical work out of the method involves (1) dividing the domain of the problem into a collection of subdomains, with each subdomain represented by a set of element

equations to the original problem, followed by (2) systematically recombining all sets of element equations into a global system of equations for the final calculation. The global system of equations has known solution techniques, and can be calculated from the initial values of the original problem to obtain a numerical answer.

Meshing is the first main problem when someone performs TCAD simulation. In order to obtain a solution of transport equation in an arbitrary geometry, one must subdivide the surface or volume in rectangular, triangular, pyramidal, etc. sub-elements with small enough sizes that the solution is locally polynomial in the region. Probably the most frequently chosen shape for the individual element is the triangle. In case of process modeling, the time and space must be partitioned in such a way so that the concentrations of the various impurities present are constant over each individual cell during each time increment along with the diffusivity and other physical parameters. Finally, the solution is computed at each discrete point, known as the mesh or grid, within the domain. The grid spacing must be sufficiently dense so that all the relevant features of the doping profile are accurately represented. The increments of time must be short enough to model important physical effects. On the other hand, it is important not to use excessively small intervals to avoid time-consuming and expensive numerical solutions.

As already stated, the layout of a mesh or grid to simulate a structure is a very important aspect of the numerical solution of the Partial Differential Equations (PDEs), as it directly determines how well the discrete model represents the actual problem. There are a number of considerations regarding grid selection. First, the points must be allocated to accurately approximate any physical quantities of interest including potentials, concentrations, fields, and currents, as well as any irregularities in the geometry of the domain. Second, because the overall computation time depends on the total number of grid points, grid points must be optimized for computational efficiency. Finally, the finer grid must be allocated in the active regions of device operation under the biasing conditions.

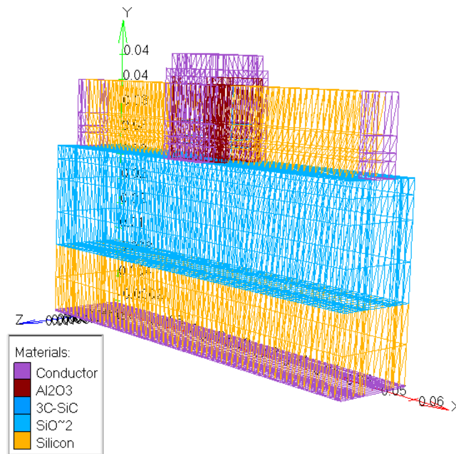

Figure 3.13 Finite element meshes (triangular elements) for 3D FinFET.

Solution variables such as potentials, doping, charge, and recombination appear in the PDEs. Therefore, high grid densities must be allocated in regions where any of these quantities undergo rapid changes (e.g., p-n junctions). Conversely, the spacing between points could be relaxed in areas where values remain relatively constant without adding a significant contribution to the overall error. In addition, the simulation structure must be robust so that the simulated device performance is independent of grid density, and the robustness of the simulation domain; that is, sensitivity of simulation results on grid must be checked after the structure generation.

3.5 Device Simulation using Atlas

The flowchart as shown in Figure 3.14 below summarizes all the processes done in device simulation using the ATLAS program from beginning up to parameter extraction. ATLAS starts by loading .str file which have been created from ATHENA. There are several steps to follow in device simulation in order to obtain the FinFET device**.** This simulation has compared the electrical characteristics between classical and quantum simulation to get exact result and proceed to optimize FinFET device. After that, this study will continue to compare some parameters with different gate lengths, doping level on channel regions, gate work functions, temperatures, gate dielectric materials. After that, the study will continue comparing some obtained parameters with those of recent research work.

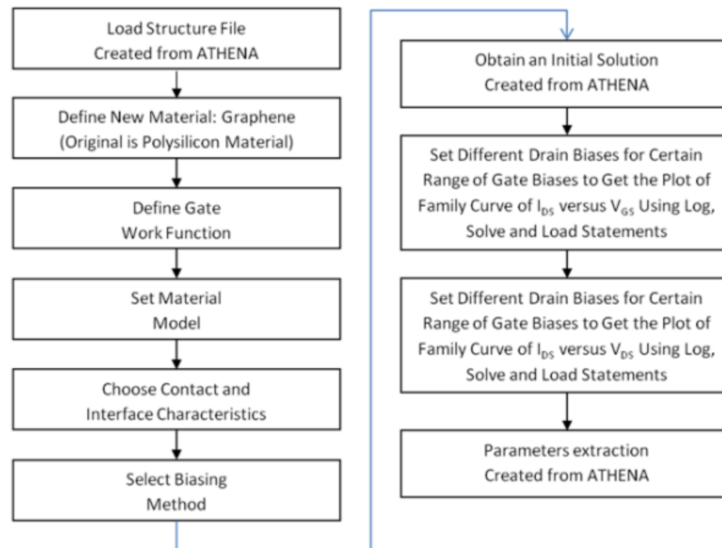

Figure 3.14 Flow chart for device simulation of n-FinFET.

3.6 Device Simulation

Device simulation start by loading **.str* created from ATHENA to ATLAS. There are several steps in device simulation in order to obtain the n-FinFET characteristics for further analysis. The output (I_{ds} versus V_{gs} curve) and (I_{ds} versus V_{ds} curve) for FinFET device will be obtained respectively. Furthermore, some parameter will be extracted, such as drain current (I_{on}), transconductance (g_m), threshold voltage (V_{th}), subthreshold swing (SS), leakage current (I_{off}), drain induced barrier lowering (DIBL), and I_{on}/I_{off} current ratio.

3.6.1 I_{DS} -V_{GS} characteristics

The choice of physical models is important to improve accuracy of the numerical simulation results. In our simulation, the inversion-layer Lombardi constant voltage and the temperature (CVT) mobility model were considered. Auger model is invoked to deal with the minority carrier recombination. The Shockley–Read–Hall (SRH) generation and recombination model have also been used. Scaling FinFET around the 8 nm technology is accompanied with great challenges. Challenges include SCE, Drain Induced Barrier Lowering (DIBL), and high leakage current. The quantum effects are rigorously taken into account in this simulation. Two numerical methods Gummel and Newton are invoked to attain the results with maximum trap 4 [4]. To generate I_{ds} versus V_{gs} characteristics curve, it is done by obtaining solutions at each step bias points first and then solving over the swept bias variable at each stepped point. For example, solutions for each V_{GS} value are obtained

with V_{ds} = 1 V. The outputs from these solutions are saved in *.log* file (solution file). For each drain bias, *.log* file is loaded and ramped the gate voltage is performed.

3.6.2 Parameters Extraction

Device parameter extraction always deal with **.log* file which contain information of I-V characteristics of device. The "extract" word in program allow the user to interpret I-V data to separate X and Y axes. From here, user can choose voltage or current for any electrode, any junction, capacitance or conductance or the transient for AC simulations. It is also allows the use for combination multiplication or division of X or Y axes to get algebraic functions.

The 3-D Poisson's equation for the channel region can be written as [2]:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}+\frac{\partial^2\varphi}{\partial z^2}=\frac{q}{\epsilon_{Si}}\,\mathrm{n_i}\,e^{\frac{q}{KT}(\varphi-\Phi_F)} \tag{3.13}$$

where q electronic charge, ϵ_{Si} permittivity of silicon, n_i intrinsic carrier density, and Φ_F non-equilibrium quasi-Fermi lever referenced to the Fermi level in the source.

The threshold voltage expression in case of a MuGFET (MultiGate Field-Effect Transistor) device structure can be expressed as [2]:

$$V_{Th}=\Phi_{ms}+2\Phi_f+\frac{Q_D}{C_{ox}}+\frac{Q_{SS}}{C_{ox}}+V_{in} \tag{3.14}$$

where Q_{ss} represents the charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents the metal-semiconductor work function difference between the gate electrode and the semiconductor and Φ_f is the Fermi potential which for P-type silicon is given by:

$$\Phi_f=\frac{KT}{q}\ln\frac{N_A}{n_i} \tag{3.15}$$

where K is the Boltzmann constant, T is the temperature, q is the electron charge, N_A is the acceptor concentration in the p-substrate, and n_i is the intrinsic carrier concentration.
when a dielectric material is inserted, the capacitance increases by the relative dielectric constant κ. In this case, the capacitance is described by eq. (3.16) [103]:

$$C_{ox}=\frac{\kappa\varepsilon_0 A}{t_{ox}} \tag{3.16}$$

where κ is the dielectric constant of the material ($\kappa = \varepsilon/\varepsilon_0$), ε_0 is the permittivity of free space, t_{ox} is the thickness of dielectric layer.

We can derive the QM threshold voltage, $V_{th,QM}$, of the MuGFET as FinFET device structure [104, 105]:

$$V_{th,QM} = V_{fb} + \psi_{s(inv)} - \frac{Q_b}{2C_{ox}} + \Delta V_{th,QM} \tag{3.17}$$

where $\psi_{s(inv)}$ is the surface potential at threshold, and $\Delta V_{th,QM}$ is the threshold voltage change due to QME's, which can be approximated as a function of the ratio of the carrier effective mass in the direction of confinement to the free electron mass and silicon film thickness which is given as [94, 105]:

$$\Delta V_{th,QM} \cong \frac{SS}{(KT/q)\ln(10)} + \frac{0.3763}{(m_x/m_0 q)T_{fin}^2} \tag{3.18}$$

where SS is the subthreshold slope and m_x/m_o is the ratio of the carrier effective mass in the direction of confinement to the free electron mass.

The critical electrical parameters such as subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are defined as [106]:

$$SS\ (mV/dec) = \frac{d\,V_{GS}}{d(\log_{10} I_{DS})} \tag{3.19}$$

$$DIBL\ (mV/V) = \frac{\Delta V_{Th}}{\Delta V_{DS}} \tag{3.20}$$

The subthreshold swing is defined as the change in gate voltage that must be applied in order to create a one decade increase in the output current. The lowest theoretical limit for SS is 60 mV/decade at room temperature [107]. The DIBL is defined as the ratio of the difference in threshold voltage measured at a low value to high value of the drain voltage [106].

The transconductance can be expressed as:

$$g_m = \frac{d\,I_D}{dV_{GS}} \tag{3.21}$$

The transconductance g_m quantifies the drain current variation due to a gate-source bias voltage variation while keeping the drain-source voltage constant [108]. Therefore, the value of g_m is extracted by taking the derivative of the I_{ds}-V_{gs} curve.

The threshold voltage (V_{th}) is a very important parameter for obtaining a higher on-current, which improves the circuit speed. Furthermore, I_{ds} is calculated as reported by the following formula [108]:

$$I_{DS}\,(nA) = 100\ \frac{W}{L}\ e^{\frac{q(V_{GS}-V_{Th})}{\eta KT}} \qquad (3.22)$$

where W is the width of the channel, L is the channel length, Q is the electronic charge, and η is the body factor, which is proportional to the change in gate voltage with a change in channel potential [108].

The leakage current is directly related to the SS. I_{off} has been calculated by the following formula [108]:

$$I_{off}\,(nA) = 100\ \frac{W}{L}\ 10^{\frac{-V_{Th}}{SS}} \qquad (3.23)$$

Transfer characteristics for considered device are illustrated in Figure 3.15. A well-behaved I-V characteristic of a 8 and 10 nm gate length TG n-FinFET device is showed in Figure 3.15. This latter compares the behaviour of the drain current respects to the gate voltage in the classical model and tacking into account the QE. The gate voltage V_{GS} is swept from 0 to 1 V in steps of 0.02 V. It can be observed that as the drain bias increases, the difference in the drain current for the same gate voltage for classical and quantum case also increases. The drain current is reduced too in the quantum case with respect to the classical case. The quantum drain current characteristics are shifted to higher gate bias for both low and high drain bias. Quantum effects modify the 3D carrier distribution in the channel, the most important effect being the shift of the charge sheet away from the interfaces into the silicon film as observed from Figure 3.15. The threshold voltage is 0.30 V for 8 nm gate length device and 0.31 V for 10 nm gate length device at V_{ds} = 0.1 V. Meanwhile, V_{DS} was chosen to see the current at conduction (inversion layer exists). The threshold voltage is extracted when I_{DS} is minimum value where the Dirac point as inversion point from hole conductance change to electron conductance (a minimum conductivity point). It is also can determine when transconductance, g_m (V_{gs}) is equal to zero. The threshold voltage obtained is an excellent value compared to the one obtained by Baravelli et al. (i.e., 0.36 V) [106]. There were some modifications at the level of the work functions of the metal gates to reach the V_{th} value desired. The conduction band splits into several subbands each of which has a minimum energy eigenvalue [109]. The quantization of energy is stronger (or equally, the separation of energy levels is higher) for thin silicon film and for larger surface electric fields. Due to the presence of the subbands, we can equivalently say that the quantum confinement raises the conduction band edge E_C to the lowest order eigenvalue. This shift has a direct influence on the device threshold voltage because it needs more band bending (potential

energy lowering) to create the inversion layer. The threshold voltage calculated both classic and quantum models which is given in table 1 with two different gate lengths. This poses an additional design challenge as the fluctuations in gate length will lead to unpredictable values of threshold voltage.

The degradation of device transconductance for quantum transport is an effect of charge set-back from interface that leads to increase in the oxide thickness. The reduced sheet density leads to an increase in the threshold voltage and a decrease in the drive current for quantum case.

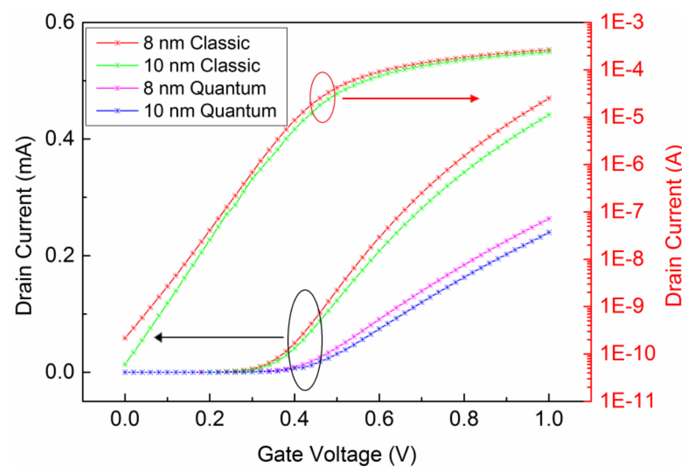

Figure 3.15 I_{ds} versus V_{gs} characteristics for two TG n-FinFET devices with different gate length at V_{ds} = 0.1 V by taking into account the BQP models in the simulation.

Table 3.1 Electrical parameters of n-FinFET device.

	8 nm	8 nm QM	10 nm	10 nm QM
V_{th} (V)	0.30	0.36	0.31	0.37
SS (mV/dec)	65.75	81.83	63.62	73.75
$G_{m\,max}$ (mA/V)	0.962	0.4967	0.8836	0.4605
$I_{d\,max}$ (mA)	0.1215	0.08086	0.1231	0.08346
DIBL (mV/V)	37.2	46.57	29.35	35.25

The threshold voltage roll-off for SOI TG FinFET decreases with reduction of gate length at the same channel thickness. The opposite are observed for the subthreshold slope, drain induced barrier lowering, and leakage current from the Table 3.1. Therefore, the transistor with the larger channel and the larger gate are the most immune to SCEs. In addition, in the strong inversion region, the quantum effects reduce the drain current as no carriers are allowed at the Silicon/ZrO_2 interface.

The Subthreshold slope and drain induced barrier lowering of the considered SOI TG

n-FinFET device with L_g = 8 nm, T_{FIN} = 4 nm, and H_{FIN} = 10 nm (i.e., 65.75 mV/dec and 37.2 mV/V) show improvement compared to TG FinFET device with L_g = 16 nm, T_{FIN} = 8 nm, and H_{FIN} = 32 nm (i.e., 70 mV/dec and 70 mV/V) [110], respectively.

At shorter channel lengths, the subthreshold slope starts to degrade because the barrier is controlled by the drain and not only by the gate. Excellent gate control on the channel potential is when the electric field lines will properly be terminated at either the two vertical gates. Thus the drain control on the channel potential is reduced leading to more immunity to DIBL. The Subthreshold slope and drain induced barrier lowering of the considered SOI TG n-FinFET device with L_g = 8 nm, T_{FIN} = 4 nm, and H_{FIN} = 10 nm (i.e., 65.75 mV/dec and 37.2 mV/V) show improvement compared to TG FinFET device with L_g = 16 nm, T_{FIN} = 8 nm, and H_{FIN} = 32 nm (i.e., 70 mV/dec and 70 mV/V) [110], respectively.

Figure 3.16 shows comparison of calculated transconductance characteristics in classical and quantum models with different gate lengths of an SOI n-FinFET device. The comparison between two gate lengths shows that the transconductance is higher for 8 nm which can be explained by the higher strain in short channel device. The peak transconductance is reduced for reducing the gate length, the highest value of 962 μA/V was extracted for the device with L_g= 8 nm at V_{ds} = 0.1 V. Shorter L_G provides less resistance and lower surface-roughness scattering which leads to a higher transconductance and mobility. It should be mentioned that the accuracy on transconductance is sometimes more important for designers that the one of the current for high quality circuit design. For g_m, the highest value of 962 μA/V was extracted for the device with L_g=8 nm. Shorter L_g provides less resistance and lower surface-roughness scattering which leads to a higher transconductance and mobility. However, reducing the gate length resulted in presence of the SCE with degradation in leakage performances of device which can be a sign of poor scalability. The BQM is more noticeable for short channel due to the higher normal electrical fields at the inversion layer in 3D.

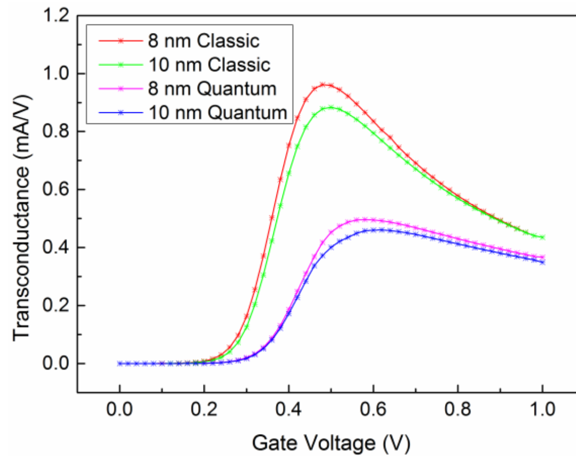

Figure 3.16 Transconductance versus V_{gs} for two TG n-FinFET devices with different gate length at V_{ds} = 0.1 V by using classical and quantum models.

Figures 3.17 and 3.18 report the output characteristics of an SOI TG n-FinFET device. The curves show the relationship between the drain current and drain to source voltage for different values of gate source voltage. First, we find that an increasing V_{GS} will result in higher channel conductivity, which means a lower channel resistivity. Some remarks can be made on the output characteristics. From the Figure 3.17, it can be easily observed that the current flattens with increasing the gate length. The current level depends on the gate length and gate voltage, which determine the number of charge carrier velocity. However, the transit time of the charge carrier from source to drain is improved with shorter gate length, which gives faster the transistor switch.

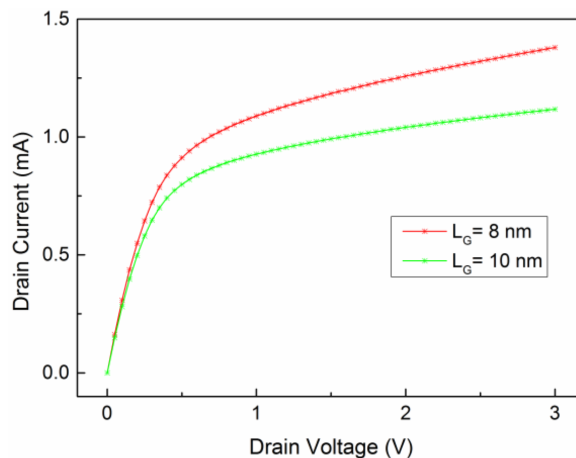

Figure 3.17 I_{ds}-V_{ds} characteristics for two SOI TG n-FinFET devices with different gate length at V_{gs} = 0.7 V.

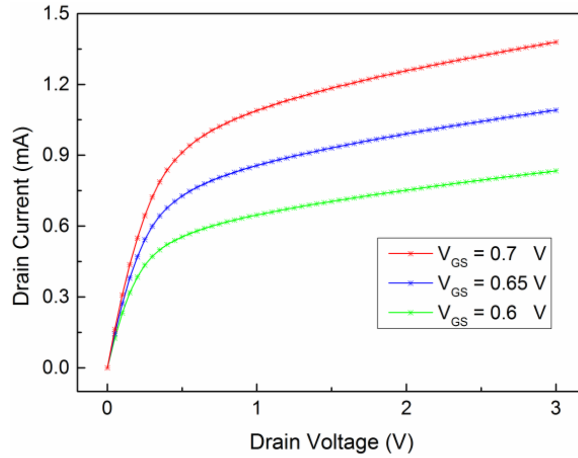

Figure 3.18 I_{ds}-V_{ds} characteristics for an SOI TG n-FinFET device with a gate length of 8 nm at three different gate-source voltages.

The change in leakage current and subthreshold slope of TG FinFET with the thin-thickness is shown in Figures 3.19 and 3.20, respectively. From the Figure 3.19, the gate voltage V_{gs} is swept from 0 to 1 V in steps of 0.02 V with $V_{gs} = V_{ds} = V_{dd} = 1$ V. From the Figure 3.19, we can distinguish the leakage current behaviour, which is the drain current when the gate voltage is zero. Figure 3.19 reports the simulated subthreshold slope of the device as a function of fin-thickness at $V_{ds} = 0.1$ V. The subthreshold slope and DIBL increase linearly with increasing fin-thickness. On the other hand, these SCEs parameters improve with decreasing of the fin-thickness as shown in the Figures 3.20 and 3.21. It should be noted that very thin-thickness improves the leakage characteristics of the device. The drain induced barrier lowering, subthreshold slope, and leakage current increase sensibly when L_g/T_{Fin} ratio is smaller than 1.5 [111, 112]. Transistor off-state current, I_{OFF} is the drain current when the gate-to-source voltage is zero ($V_{gs}= 0$ V). There are many factor that can influence I_{OFF} such as V_{th}, channel physical dimensions, channel / surface doping profiles, drain / source junction depth and gate oxide thickness and V_{dd}. The other current that flows between source and drain when transistor is in the on-state, is called I_{ON} which defined as maximum value of I_{DS}. The on-current output at $V_{dd} = V_{gs} = V_{ds} = 1$ V with a gate length of 8 nm is 2.85 mA. It decreases low to 2.52 mA increasing the gate length at 10 nm. The leakage current is directly related to the SS. The leakage current output is 572 pA and 202 pA with a 8 nm and 10 nm gate length respectively when the working point is fixed at $V_{gs} = 0$ V and $V_{dd} = V_{ds} = 1$ V. The leakage current and subthreshold slope of the considered device (i.e., 572 pA and 65.75 mV/decade) are very good compared with the results of the recent paper [113], reporting on a gate-all-around MOSFET with $L_g = 20$ nm, $T_{FIN} = 12$ nm, $H_{FIN} = 24$ nm (i.e., 700 pA and 86.73 mV/dec), even with a smaller physical L_g. It is important to keep I_{off} very

small, in order to minimize the static power dissipation even when the system or device is in the standby mode. All the minimum values of these device parameters are required for small size of the transistor. Furthermore, transistor dimensions scale to minimize parasitic capacitances, to reduce power consumption, and to improve current drive and circuit speed. The ratio I_{on}/I_{off} exceeds 10^6 for the analyzed device with ZrO_2 as gate dielectric material at room temperature, which indicates the excellent on-state and off-state characteristics compared with the results of the recent paper reporting on a 20 nm conventional FinFET (i.e., 7.42 10^3) [115]. The simulations were carried out setting the device temperature at T = 300 K by keeping the fin thickness minimum (≈ $L_g/2$).

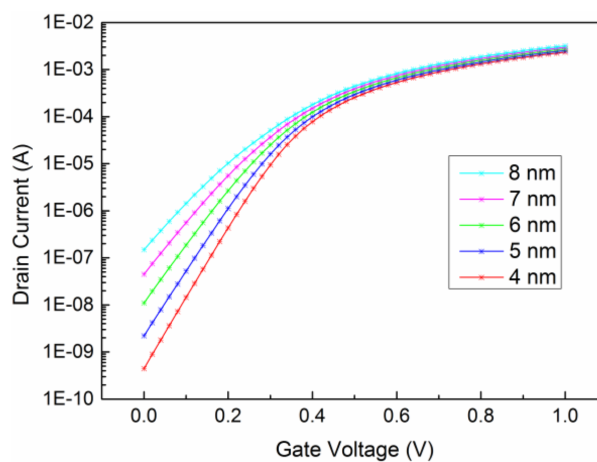

Figure 3.19 I_{ds}-V_{gs} characteristics on a log scale for an SOI TG n-FinFET device with different fin thickness at V_{ds} = 1 V and L_g = 8 nm.

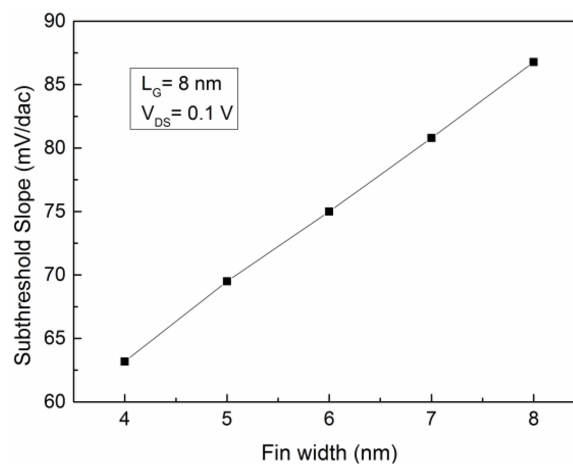

Figure 3.20 Subthreshold slope variation for different fin thickness of n-FinFET at V_{ds} = 0.1 V and L_g = 8 nm.

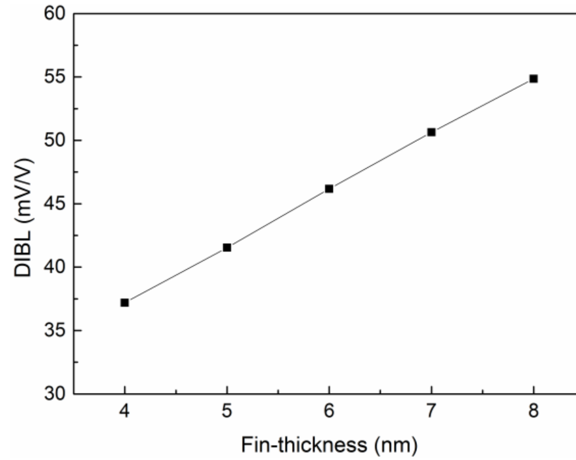

Figure 3.21 DIBL variation for different thin-thickness of n-FinFET device.

The ratio I_{on}/I_{off} exceeds 10^6 for the analyzed device with ZrO_2 as gate dielectric material at room temperature, which indicates the excellent on-state and off-state characteristics. The simulations were carried out setting the device temperature at T = 300 K by keeping the fin thickness minimum ($\approx L_g/2$).

Figure 3.22 shows a typical curve of drain current versus gate voltage characteristics in logarithmic scale of tri-gate n-FinFET for different values of the gate work functions where the V_{ds} value is 1 V. From the figure, we can observe that the leakage current differences increase with increasing the Φ_m value. Figure 3.23 presents the simulated threshold voltage of the device as a function of Φ_m at V_{ds} = 0.1 V. The threshold voltage increases linearly with Φ_m value.

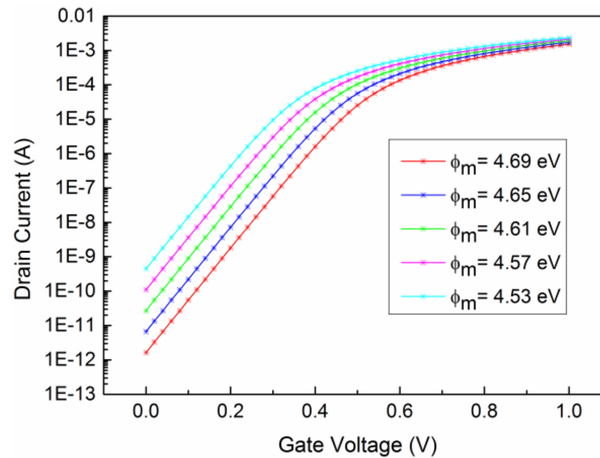

Figure 3.22 I_{ds}-V_{gs} characteristics on a log scale for an SOI TG n-FinFET device with different gate work function at V_{ds} = 1 V and L_g = 8 nm.

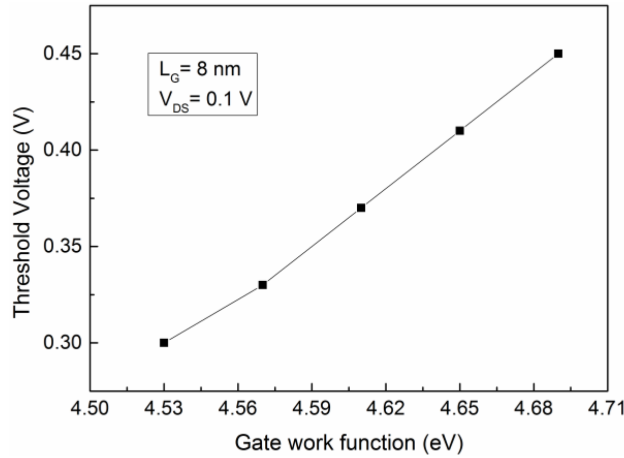

Figure 3.23 Threshold voltage versus gate work function of n-FinFET and L_g = 8 nm.

3.6.3. Effects of variations of the channel doping concentration

In this section we investigate the impact of channel engineering on TG n-FinFET by using different channel doping. From the results it is observed that we can improve the short channel effects by changing the channel doping. The impact of channel engineering also observed on performance parameters of the TG n-FinFET such as subthreshold slope, transconductance, on-current, I_{on}/I_{off} current ratio, and carrier mobility. Thus, an optimized value of the channel doping will be projected for future reference in context of leakage power and the channel engineering will play an important role in optimizing the device parameters. Threshold voltage of the device is an important parameter which decides the device performance. The value of gate to source voltage (V_{gs}) for which sufficient amount of mobile electrons accumulates in the channel region, so that a conducting channel is formed, is called the threshold voltage. A well-behaved I-V characteristic and transconductance with different channel doping concentration of TG n-FinFET device is demonstrated in Figure 3.24. Figure 3.25 shows the variation of threshold voltage and subthreshold swing with different doping levels.

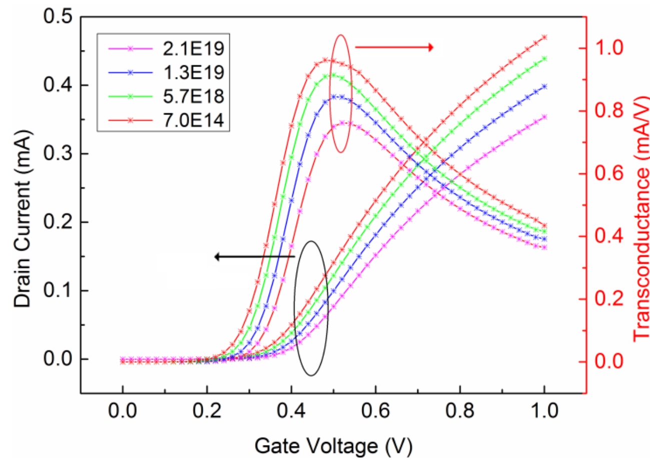

Figure 3.24 I_{ds}-V_{gs} characteristics on a linear scale for an SOI n-FinFET device at different channel doping.

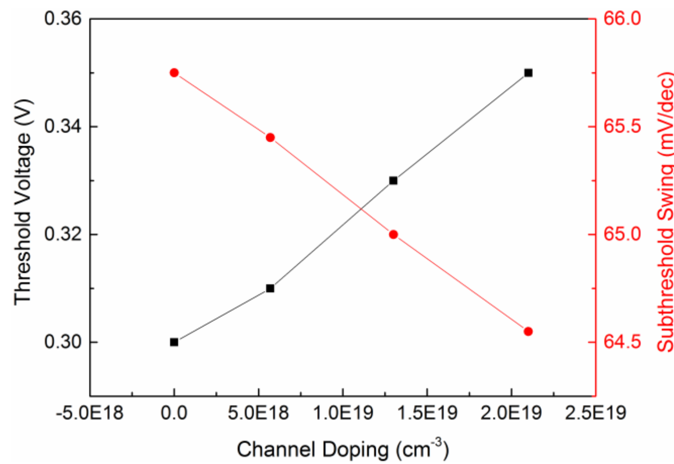

Figure 3.25 Threshold voltage and subthreshold swing versus Channel doping concentration.

From Figures 3.24 and 3.25, it is clear that as we increase the channel doping linear as well as threshold voltage of the device increases. So we can have desired value of the threshold voltage by varying the channel doping. But high channel doping cannot be done as it leads to band to band tunneling and gate induced drain leakage [111]. The suitable value of channel doping is around 1.0E16 cm^{-3} and value of threshold voltage at this doping level are 0.3 V (linear threshold voltage) which is optimum value of threshold voltage for the gate length of 8 nm. As we increase the channel doping, subthreshold swing increases linearly as shown in Figure 3.26. Lower value of subthreshold swing is desirable so undoped or lightly doped channel devices are preferred over doped channel devices.

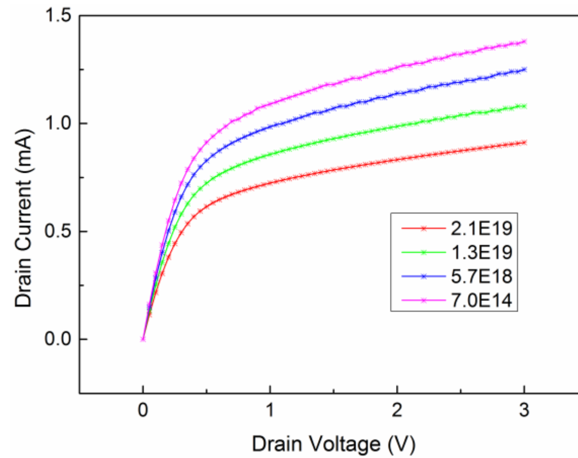

Figure 4.26 I_{ds}-V_{ds} characteristics for an SOI n-FinFET at different channel doping levels.

The On-current, decides the driving capability of the device. It is defined as drain to source current when $V_{gs}=V_{ds}=V_{dd}$ and V_{dd}= 1V. Figure 3.27 given below show the drive current and maximum transconductance variation for different doping levels.

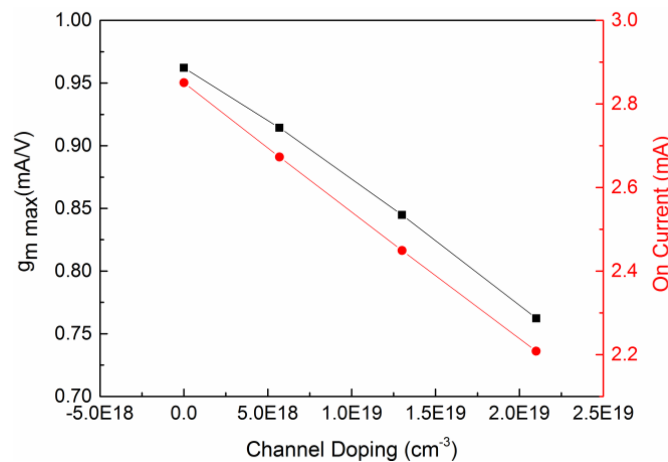

Figure 3.27 Transconductance and on-current versus channel doping concentration.

With the increasing of channel doping, the value of threshold voltage increases; as a result the on-current and the transconductance get decrease. Figure 3.27 shows approximately linear variation of transconductance and on-current with channel doping.

DIBL effect occurs in short-channel devices when the depletion regions of the drain and the source interacts each other near the channel surface lowering of the source potential barrier height. Appling the drain voltage, the barrier height reduces due to the influence of drain electric field. This leads to injection of more carriers in the channel region but this increase in the carrier is due to the drain voltage and not to the gate voltage. DIBL is more prominent at high drain voltages and shorter channel lengths. We can reduce drain induced

barrier lowering effect by using higher surface and channel doping [25, 42]. From Figure 3.28 we can see that as we increase the channel doping, the number of carrier in channel region increases and DIBL value reduces.

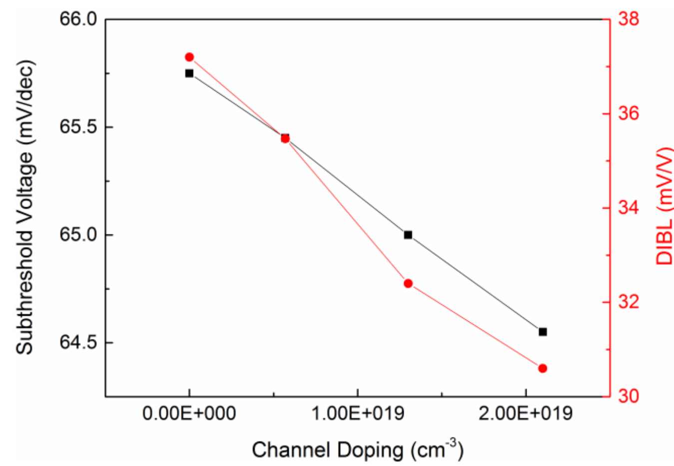

Figure 3.28 Subthreshold swing and DIBL versus channel doping concentration.

FinFET's drain leakage current is defined as drain to source current when V_{gs}= 0 V and V_{ds} = V_{dd}. FinFET's drain leakage current or off-current (I_{off}) is the drain current when no gate voltage is applied. This off-current is influenced by several other parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide, channel/surface doping profile and supply voltage (V_{DD}). In our case this latter parameter is fixed at 1V. As the device dimensions are shrinking, leakage currents are becoming as one of the major parameter which needs more attention. In long channel devices off-state current is mainly due to leakage from the drain-well and well-substrate reverse-bias p-n junctions [7]. Figure 3.29 presents I_{ds}-V_{gs} characteristics on a log scale with different doping levels. From this figure, it can be seen that the leakage current deceases with increase of the doping.

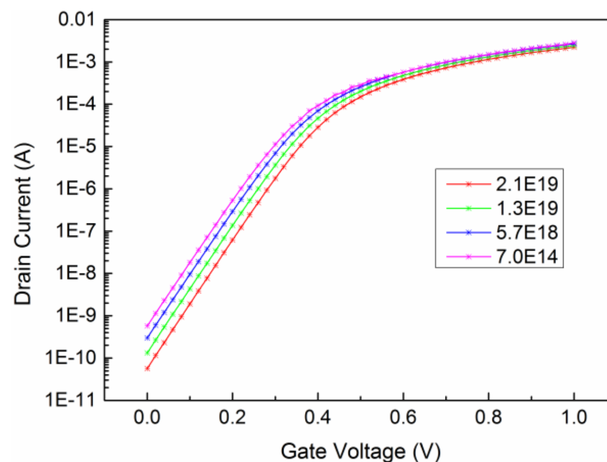

Figure 3.29 I_{ds}-V_{gs} characteristics on a log scale for an SOI TG n-FinFET device with different channel doping at V_{ds} = 1 V and L_g = 8 nm.

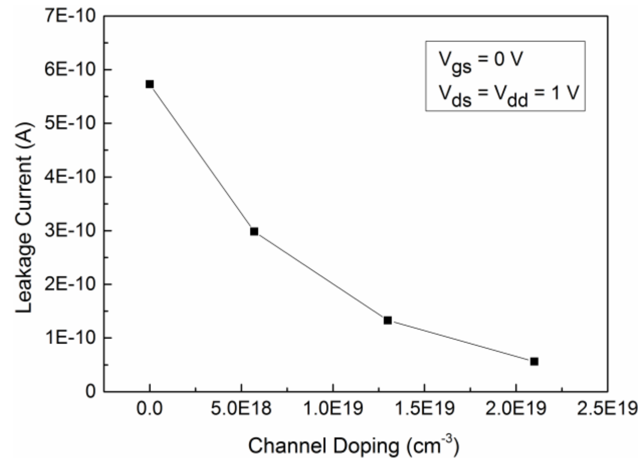

Figure 3.30 Leakage current versus channel doping concentration.

With increase in channel doping off-current get reduces. Figure 3.31 shows the curve between leakage current versus channel doping, from this we can see that for higher values of channel doping off-current get reduces very sharply. The I_{on} is the maximum current at gate voltage V_{ds}=V_{dd}. The I_{on}/I_{off} current ratio represents the power consumption of a device.

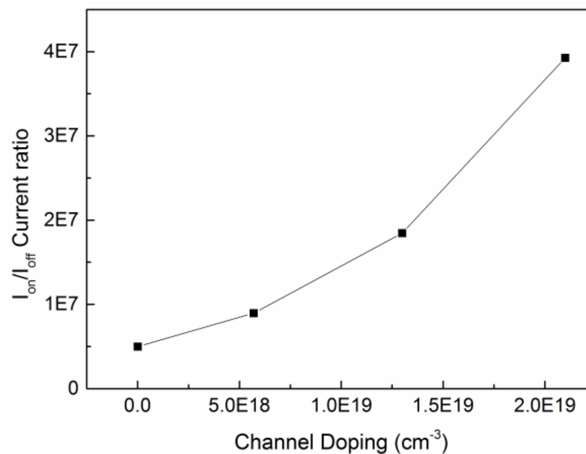

Figure 3.31 log (I_{on}/I_{off}) versus Channel doping concentration.

As we increase the channel doping, the drive current reduces almost linearly but the off-current decreases exponentially. This leads to a very sharp increase of the I_{on}/I_{off} ratio. It can be noticed from the results, that the device behaviour changes only when the value of the donor doping approaches to the value of the acceptor doping. At this doping level, the device allows current to flow from drain to source when the gate voltage is less than the threshold voltage. At voltages higher than this, the device allows no current to flow from drain to source as shown in Figure 3.32.

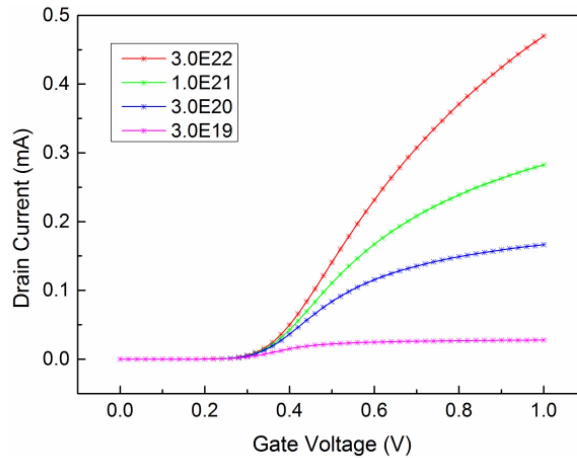

Figure 3.32 I_{ds}-V_{gs} characteristics on a linear scale for an SOI n-FinFET device at different Drain/Source doping (Donor doping).

One primary goal of optimization is to achieve a low threshold voltage. A lower threshold voltage for the device means that it can be applied to low voltage working applications. If the device can be operated at a lower voltage, it will use less power, making it more attractive yet.

Another goal is a high transconductance: the higher the transconductance the closer to ideal the device will perform. Also, if the device has a steep threshold slope, it will switch faster, making it more suitable to digital logic design.

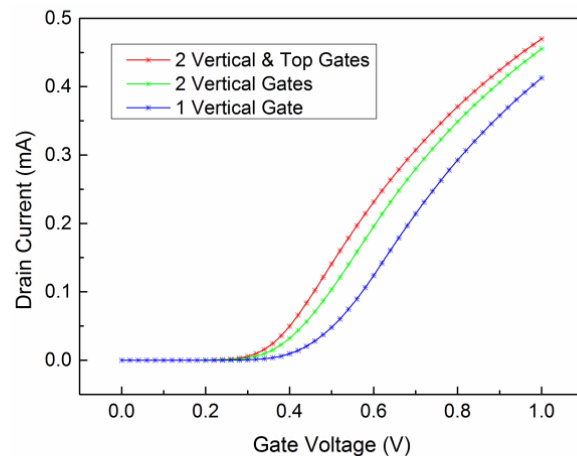

Figure 3.33 I_{ds}-V_{gs} characteristics on a linear scale for an SOI n-FinFET device at different gates.

From the Figure 3.33 it may be inferred that a better control of the channel can be achieved using three gates. Figure 3.33 shows an example where one vertical gate of the device was biased with V_{ds}= 0.1 V and performs a threshold of about 0.4 V. In the example, if both vertical gates were biased, the device would clearly be "on" and the current will flow

through the device. This allows for a dynamic threshold voltage that is dependent on the voltage applied to both gates. It is noticed that when we apply a voltage of top gate with two vertical gate there will result a change in characteristics such us threshold voltage, tranconductance, and on-current.

From the above discussions, we can conclude that as we scale down the devices, threshold voltage of the device decreases. To adjust the threshold voltage and other short channel effects within the permissible limits we can do channel engineering, but we cannot increase the channel doping beyond a certain limit because of the behaviour of some parameters like subthreshold swing and drain induced barrier lowering. If we increase channel doping one parameter get improved while other get worse. Therefore, we have to optimize their value at particular doping level. We also cannot use high doping because mobility degradation of carrier takes place in the channel region.

3.6.4. Effects of variations of the gate metal work function

Figure 3.34 presents a FinFET structure with different parameters compared to the previous structure. It is very useful to consider the impact of the gate metal work function Φ_m on the device current and performances. Figure 3.36 illustrates the transfer characteristics when Φ_m ranges from 4.5 eV to 4.8 eV in the considered device. We can observe that, when the gate work function increases, the threshold voltage increases too and the drain current characteristic slope decrease as shown in Figures 3.35 and 3.36. The schematic structure used for the simulations is represented in Figure 3.34. The different parameters of the considered structure are listed in Table 3.2:

Table 3.2. Parameters of symmetrical SOI n-FinFET

Symbol	Designation	Value
L_d, L_s	Drain length and Source length	11 [nm]
L_g	Gate length	8 [nm]
T_{ox} (Si_3N_4)	Lateral oxide thickness (gate dielectric material)	1 [nm]
T_{FIN}	Silicon thickness	4 [nm]
H_{FIN}	Fin Height	10 [nm]
T_{Box} (SiO_2)	Buried oxide thickness	15 [nm]
$T_{Substrate}$	Substrate thickness	10 [nm]
N_A	Channel concentration	10^{16} [cm^{-3}]
N_D	Drain and Source concentration	10^{20} [cm^{-3}]

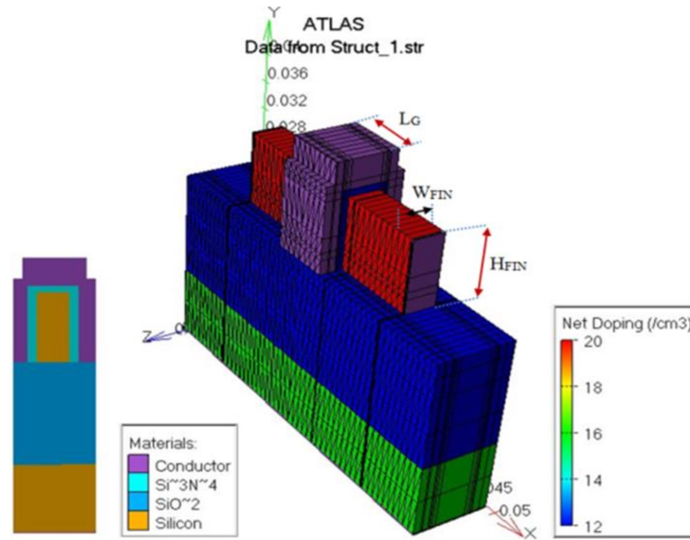

Fig. 3.34 Illustrates the device structure of an n-FinFET in 3-D with a gate length of 8 nm.

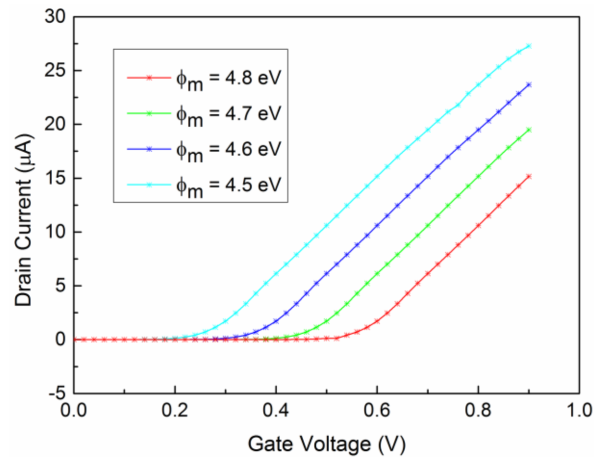

Figure 3.35 I_{ds}-V_{gs} characteristics on a linear scale for an SOI n-FinFET with different values of Φ_m at $V_{ds} = 0.2$ V.

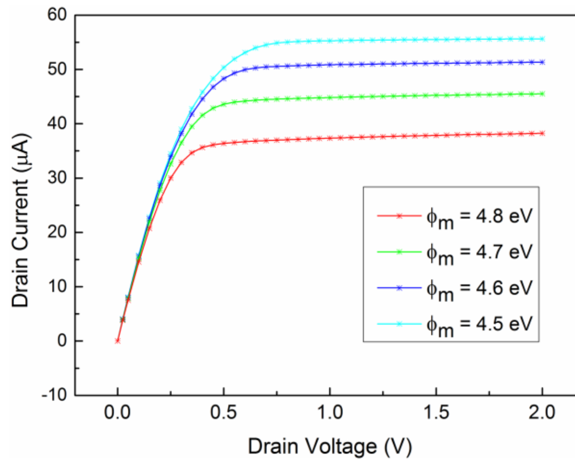

Figure 3.36 I_{ds}-V_{ds} characteristics for an SOI n-FinFET at different values of Φ_m.

In Figure 3.38, it is observed that the subthreshold slope does not change with the variation of the gate work function. According to the relationship between I_{off} and V_{th} reported in eq. 3.23, the threshold voltage increases with a higher metal gate work function, which in turn causes a reduction in the leakage current as shown in Figure 3.39.

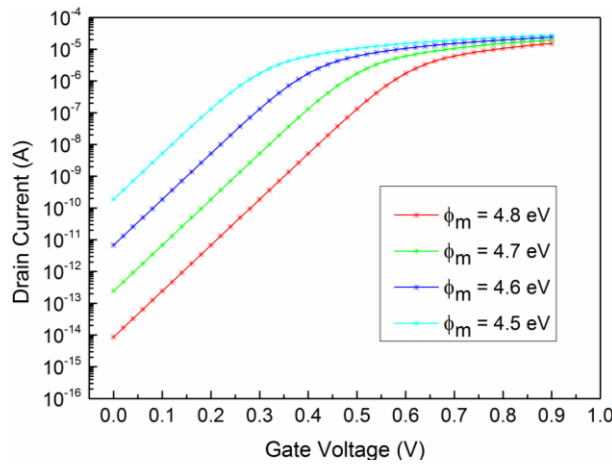

Figure 3.37 I_{ds}-V_{gs} characteristics on a log scale for an SOI n-FinFET with different values of Φ_m at $V_{ds} = 0.2$ V.

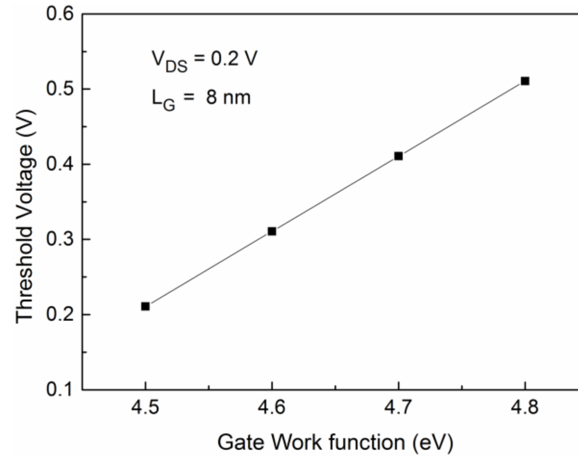

Figure 3.38 Threshold voltage versus gate work function of n-FinFET.

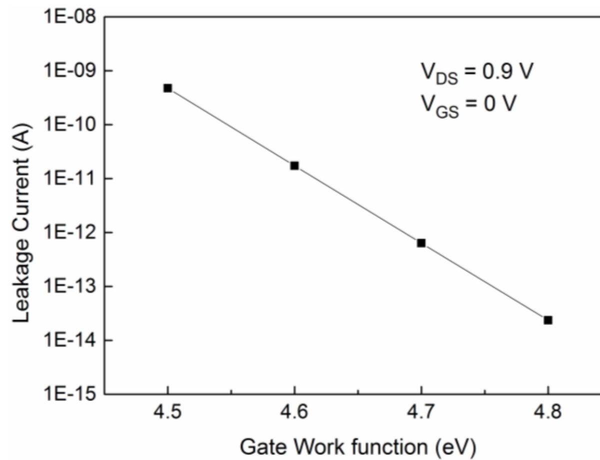

Figure 3.39 Leakage current versus gate metal work function for an n-FinFET.

From Figure 3.40, we can notice that the on-current decreases as Φ_m is increased and again, as shown in Figure 3.41. The on/off current ratio improves with an increase of Φ_m. Figure 3.42 shows that a low value of the gate metal work function leads to a higher g_m value, and a higher drain current as shown in Figure 3.42. According to the relationship in eq. 3.21, g_m is directly related to the drain current (I_d). Therefore, we can conclude that the work function has a very notable effect on the threshold voltage, the transconductance, the leakage current, the on-current and the on/off current ratio.

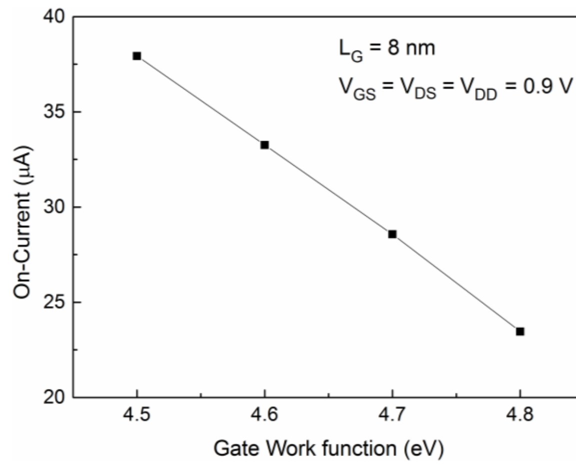

Figure 3.40 On-current variation with different gate metal work function values.

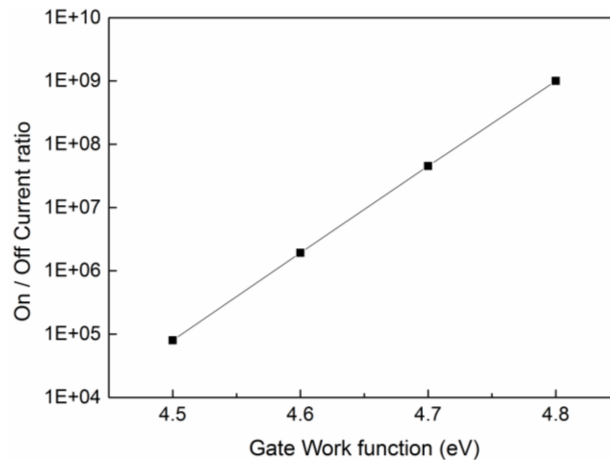

Figure 3.41 On/off current ratio versus gate metal work function.

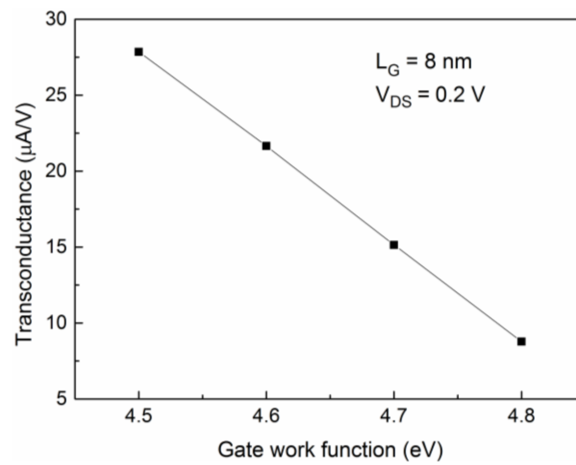

Figure 3.42 Transconductance versus gate metal work function.

3.6.5. The effects of gate dielectric material on electrical characteristics of n-FinFET device

In the following paragraph, we present an investigation of the electrical characteristics of a nanoscale SOI tri-gate n-channel fin field-effect transistor (FinFET) structure with 8 nm gate length using zirconium dioxide (ZrO_2) as gate dielectric material. The numerical device simulator ATLAS™ is used to simulate the structure in three dimensions with different models. The drain current, transconductance, threshold voltage, subthreshold swing, leakage current, drain induced barrier lowering, and on/off current ratio are analysed in the various biasing configuration. FinFET device with a high value of gate dielectric constant exhibits much better performance compared to the Si_3N_4 dielectric material. It is found that increasing the k value was beneficial in reducing the subthreshold slope, drain induced barrier lowering, and leakage current. In addition, the temperature dependence of the main electrical parameters of the SOI tri-gate n-FinFET is analysed. Increase of temperature tends to worse some basic parameters, such as subthreshold slope, transconductance, on-current, leakage current, and on/off current ratio.

3.6.5.1. Device structure

The 3D schematic view of the simulated TG FinFET structure is shown in Figure 3.43. The device dimensions, L_g, H_{FIN}, T_{FIN}, and t_{ox} are the gate length, the height of silicon fin, the thickness of silicon fin, and the thickness of gate oxide respectively. The thin ZrO_2 layer has been proposed to replace conventional SiO_2 gate dielectric material for good gate control of SCE. In TG FinFET, as depicted in Figure 3.43, the gate oxide thickness is equal in all three sides of the fin region and it has been fixed at 1.5 nm. The height of silicon fin (H_{FIN} = 10 nm) is defined as the distance between the top gate and bottom gate oxides. The thickness of silicon fin (T_{FIN} = 4 nm) is defined as the distance between front gate and back gate oxides [4]. The channel region is formed by a slightly doped volume with doping concentration 10^{16} cm^{-3} (P-type). The doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3} (n-type). The value of the gate work function is 4.53 eV.

3.6.5.2. Device simulation using Silvaco-Atlas

The numerical device simulator, ATLAS™ has been used to simulate the structure of the proposed SOI TG n-FinFET with high-k material. The choice of physical models is important to improve accuracy of the numerical simulation results. In our simulation, the

Lombardi's inversion-layer constant voltage and temperature (CVT) mobility model was considered [113]. Auger model is invoked to deal with the minority carrier recombination. The SRH generation and recombination model have also been used. Two numerical methods Gummel and Newton are invoked to attain the results [4].

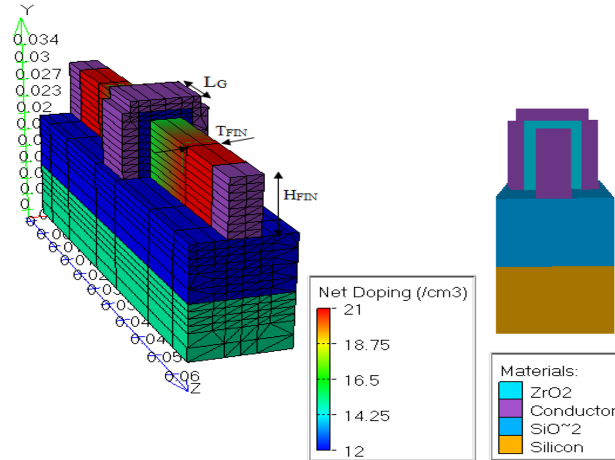

Figure 3.43 Illustration the SOI TG n-FinFET structure.

The gate dielectric materials play a key role in the design of novel and high performances at nanoscale of electrical devices. It is well known that high-κ materials are more suitable than the well-known SiO_2 due to the smaller thickness required which decreases the threshold voltage and improves the leakage characteristics of the device. This simulation has been performed for three different gate dielectrics which are silicon nitride (Si_3N_4, κ = 7.55), aluminum oxide (Al_2O_3, κ = 9), and zirconium dioxide (ZrO_2, κ = 25) **[78]**. The dependencies of SS and DIBL on the gate dielectric constant for TG n-FinFETs are shown in Figures 3.44 and 3.45, respectively. Initially, subthreshold slope decreases with increase of gate dielectrics constant. Afterwards, slope starts decreasing and comes close to its theoretical limit, which is shown in Figure 3.44. This observation indicates that, higher value of gate dielectrics gate is desired in order to have fast n-FinFET response. Furthermore, DIBL and leakage current decrease as gate dielectric constant decreases as shown in Figures 3.45 and 3.46, respectively. During accurate circuit design, the first important step is to get rid from these DIBL effects of the transistor.

Figures 3.47 and 3.48 illustrate the on-current and on/off current ratio characteristics with different gate dielectric constants for an SOI TG n-FinFET, respectively. I_{On} is also significant for device performance. Furthermore, the variation of transconductance with different gate dielectrics at the gate-source voltage V_{GS} for which $g_{m\ max}$ is simulated. It can be seen that transconductance increases with the increase of dielectric constant as shown in

Figure 3.49. All these characteristics improve with an increase of dielectric constant κ, we can observe that the best results are obtained when ZrO_2 is used as a gate dielectric.

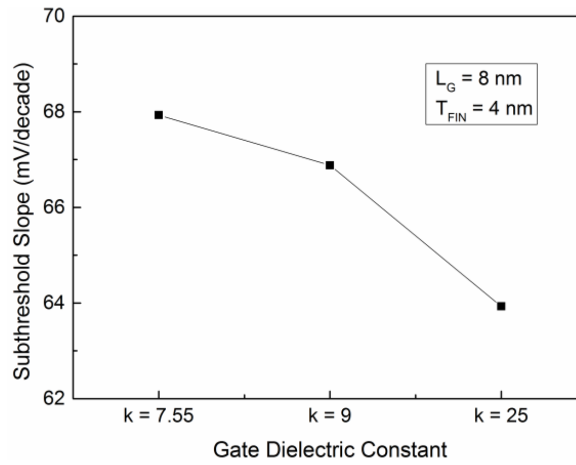

Figure 3.44 Subthreshold slope variation for different gate dielectrics at V_{ds} = 0.1 V.

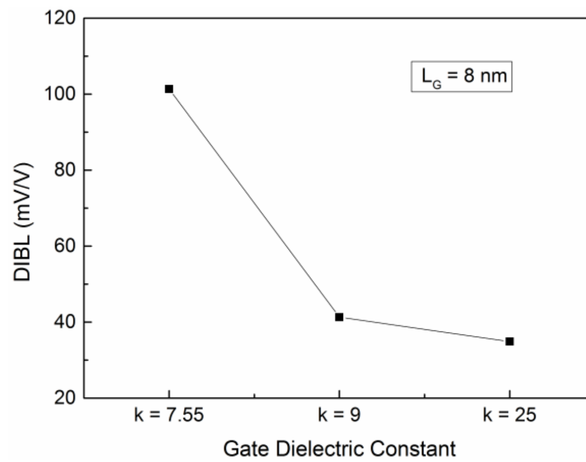

Figure 3.45 DIBL variation for different gate dielectrics.

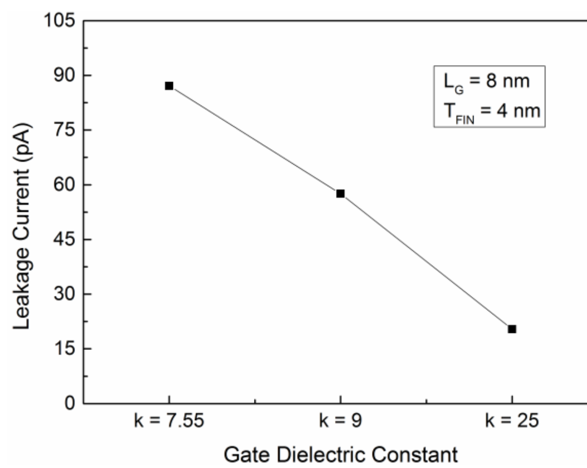

Figure 3.46 Leakage current variation for different gate dielectrics at $V_{gs}= V_{ds}$ and V_{ds} = 1 V.

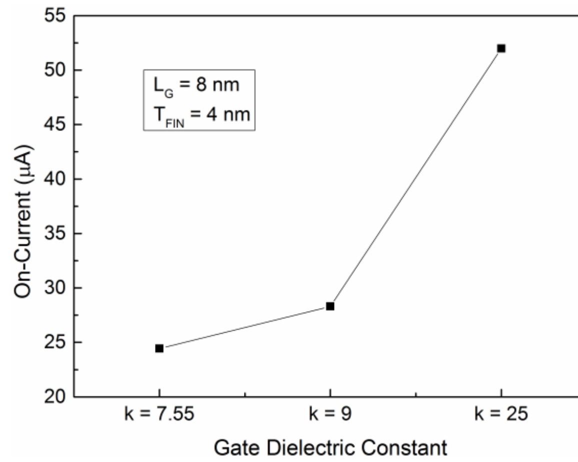

Figure 3.47 On-current variation for different gate dielectrics at $V_{gs}= V_{ds}$ and V_{ds} = 1 V.

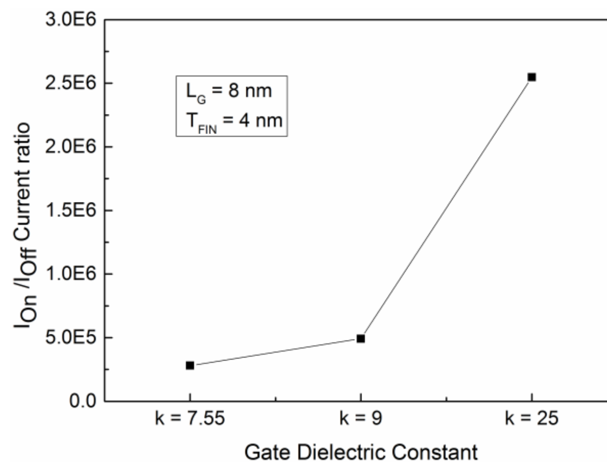

Figure 3.48 I_{On}/I_{Off} current ratio for different gate dielectrics.

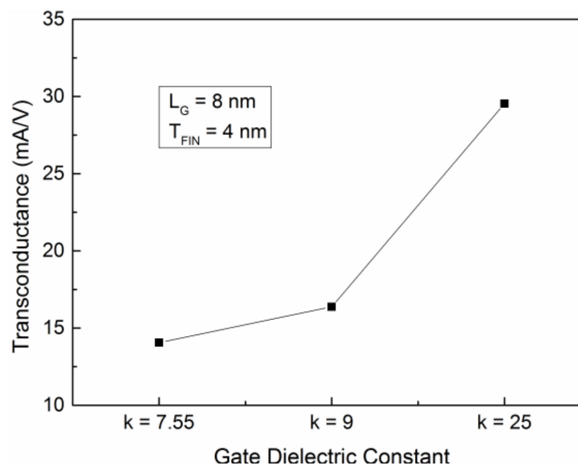

Figure 3.49 Maximum transconductance variation for different gate dielectrics at V_{ds} = 0.1 V.

3.6.6. The effects of temperature on electrical characteristics of n-FinFET device

In Figures 3.50 and 3.51, I_{ds}-V_{gs} transfer characteristics at different temperatures are shown on a linear and log scale for the TG n-FinFET device structure at V_{ds} = 0.1 V. The temperature is changed from 30°C to 200°C. The threshold voltage decreases and the subthreshold slope increases almost linearly in the device as temperature is increased. Figures 3.52 and 3.53 present the simulated threshold voltage and subthreshold slope of the device as a function of temperature at V_{ds} = 0.1 V, respectively. The threshold voltage for different temperatures matches perfectly. In a FinFET device, the decrease of threshold voltage with temperature tends to increase drain current in weak inversion while the mobility reduction gives rise to a decrease in strong inversion [114, 115]. There exists a gate bias point at which these opposing effects compensate one another, called the "zero temperature coefficient" (ZTC) point [116, 117]. Basically, there two ZTC points for a transistor, one for the drain current and the other for transconductance, and in general they have different values in linear and saturation regions. The ZTC point of the drain current is around V_{gs} = 0.52 V for n-channel FinFET device in Figure 3.50 [118]. Figure 3.54 shows transconductance characteristics as a function of gate voltage where ZTC is around V_{gs} = 0.52 V with various temperatures in device with W = 4 nm and L_g = 8 nm at V_{ds} = 0.1 V. The simulated transconductance exhibits roughly the same shape with different maximum value at different temperatures. In particular, the transconductance first increases and then decreases by increasing the gate voltage at V_{ds} = 0.1 V, as shown in Figure 3.54. Moreover, the maximum transconductance decreases with the increase of temperature. The temperature dependence of output I_{ds}-V_{ds} characteristics is shown in Figure 3.55. The on-current of TG n-FinFET device decreases with temperature as gate bias is larger than ZTC bias, as shown in Figure 3.56. From the simple expression for the saturated drain current in a FET transistor, eq (3.24) can be expressed in the following way when temperature dependence of the electron mobility and threshold voltage are included:

$$I_d = I_{d,sat} = \frac{W}{L}\ \mu(T) C_{ox}\ \frac{\left(V_{gs} - V_{th}(T)\right)^2}{2n} \tag{3.24}$$

For small values of gate voltage and correspondingly small current, the threshold voltage term dominates, and the decrease in threshold voltage with increasing temperature results in a positive temperature coefficient for saturation current, that is, the saturation current increases with temperature. For large gate voltages, the negative temperature

coefficient of the mobility term dominates, and saturation current decreases with temperature. the saturation current does not change with temperature, as is shown in Figures 3.50 and 3.54. The ZTC point arises from the cancellation of the opposite thermal dependences of the threshold voltage and the electron mobility. Increase of temperature drives the increase of intrinsic carrier concentration in silicon, which caused increase of leakage current while tends to exhibit degradation to ratio I_{on}/I_{off} as is illustrated in Figure 3.60 [119, 120]. The evolution of leakage current of considered device is shown in Figures 3.56 and 3.57. Furthermore, Figure 3.59 illustrates sensitivity of DIBL to temperature.

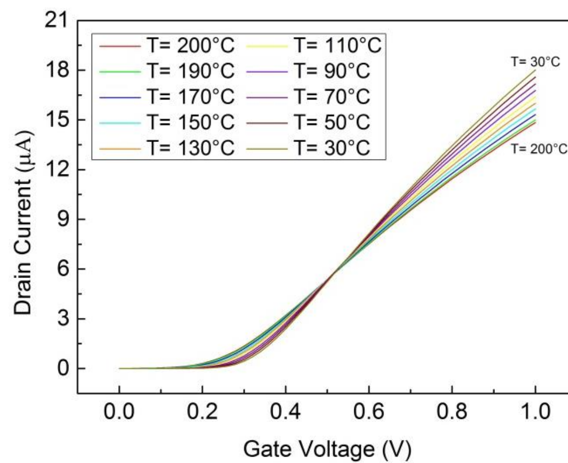

Figure 3.50 Linear scale of I_{ds} versus V_{gs} at different temperatures at V_{ds} = 0.1 V.

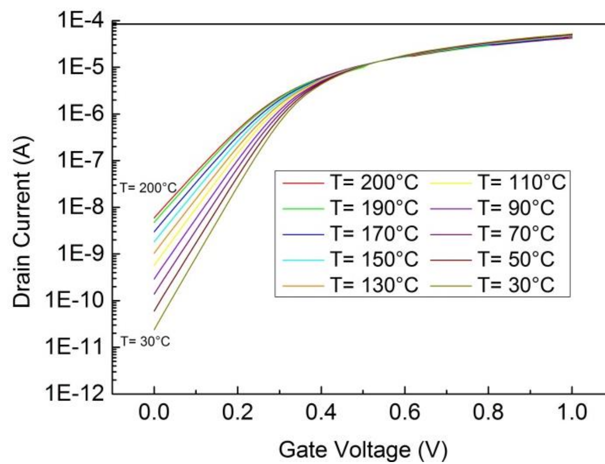

Figure 3.51 Log scale of I_{ds} versus V_{gs} at different temperatures at V_{ds} = 1 V.

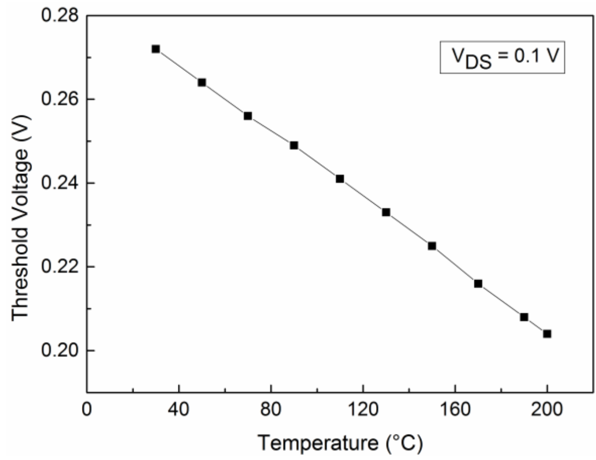

Figure 3.52 Threshold voltage of TG n-FinFET as a function of temperature with V_{ds} = 0.1 V.

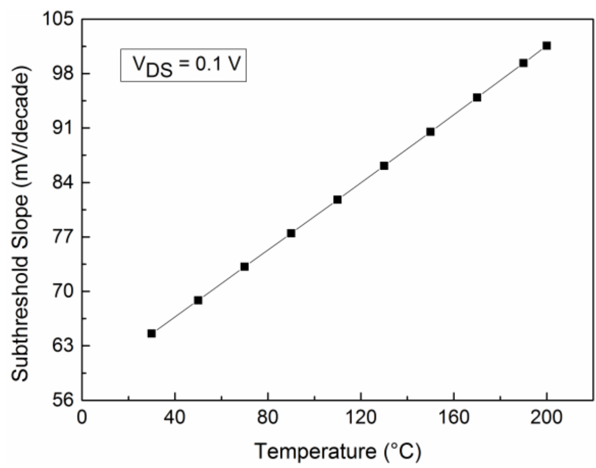

Figure 3.53 Subthreshold slope of TG n-FinFET as a function of temperature with V_{ds} = 0.1 V.

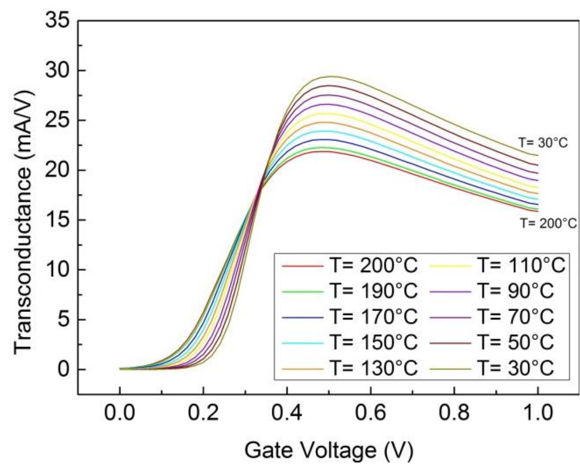

Figure 3.54 Transconductance characteristics with various temperatures at V_{ds} = 0.1 V.

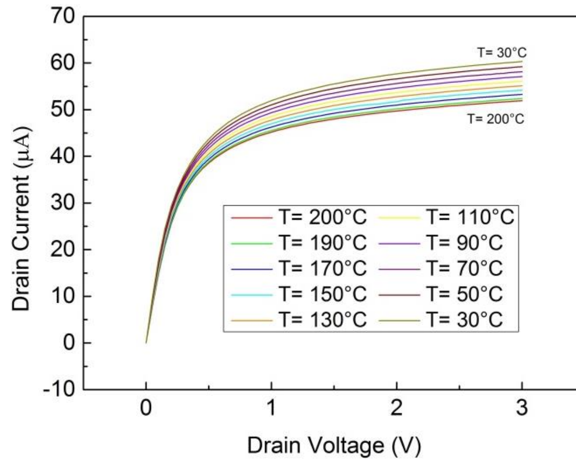

Figure 55 Linear scale of I_{ds} versus V_{ds} at different temperatures at $V_{gs} = 0.9$ V.

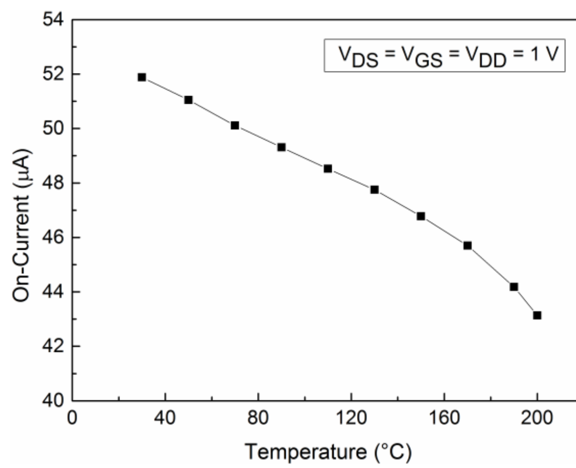

Figure 3.56 On-current of TG n-FinFET as a function of temperature with $V_{ds} = 1$ V.

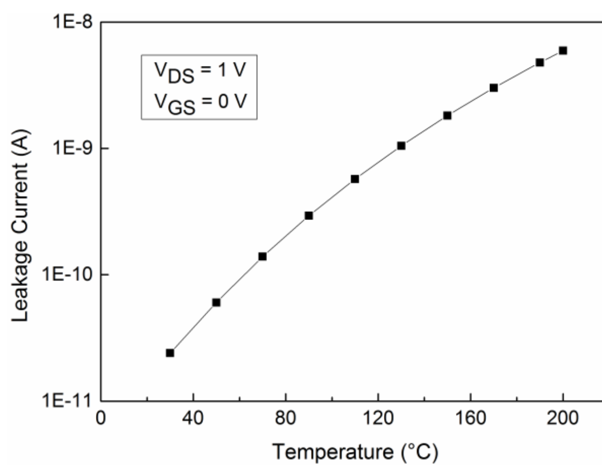

Figure 3.57 Leakage current of TG n-FinFET as a function of temperature with $V_{ds} = 1$ V and $V_{gs} = 0$ V.

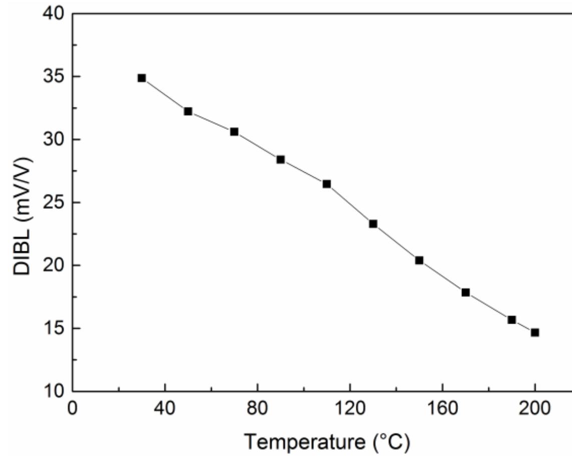

Figure 3.58 DIBL of TG n-FinFET as a function of temperature at $V_{ds} = 0.01$ V (V_{ds} Low) and $V_{ds} = 0.05$ V (V_{ds} High) of the SOI TG n-FinFET device.

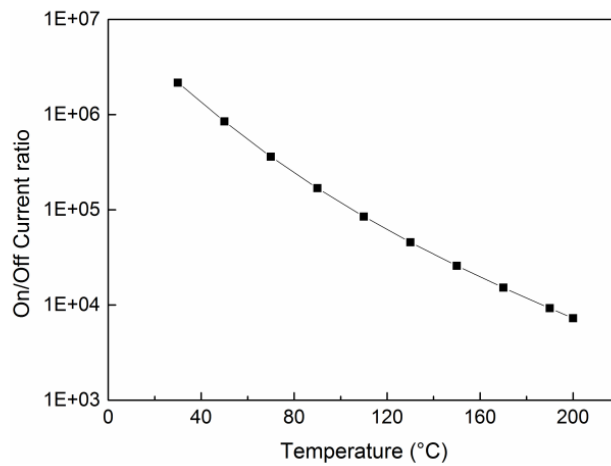

Figure 3.59 On/off current ratio of TG n-FinFET as a function of temperature.

3.6.7. Effect of Number of fins on electrical device characteristics

The FinFET structure is based on a vertical silicon fin characterized by the gate length, fin height (H_{FIN}), and the silicon thickness as shown in Figure 3.60 [4]. The channel region is formed by a slightly doped volume with doping concentration 10^{16} cm^{-3} (p-type). The doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3} (n-type). The thin Al_2O_3 layer has been used to replace conventional SiO_2 gate dielectric material for good gate control and to improve the reliability and the mobility of the device below the two vertical gates. At the top corners of FinFETs, the generation of parasitic inversion channel can be eliminated by using Si_3N_4 hard mask below the single gate on top of the device **[4]**. The value of the gate work function is 4.6 eV.

Figure 3.60 shows the structure of a multi-fin n-FinFET where each fin is separated

from the other fin by a minimum pitch of 6 nm **[2]**. The purpose of the multiple fin use is to increase the drain current. This has been confirmed by the simulations done with Silvaco.

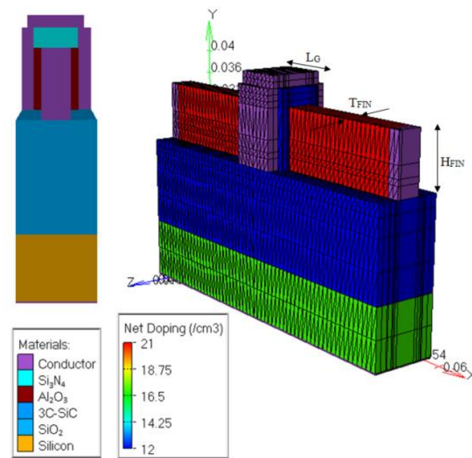

Figure 3.60 The device structure of a SOI n-FinFET.

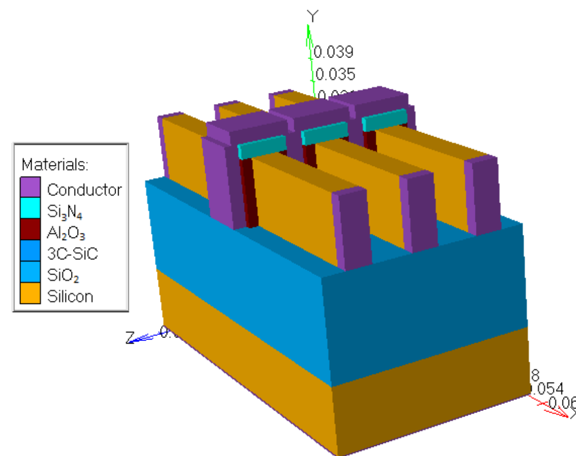

Figure 3.61 The device structure of a 3-fin device.

To making smaller transistors possible, FinFETs also might conduct electrons at least five times faster than conventional silicon transistors, called MOSFETs, or metal-oxide-semiconductor field-effect transistors. The FinFETs could enable industry to not only create smaller devices, but also much faster computer processors. Connecting FinFET in parallel will increase the current handling capability of the circuit when used as a switch, so here we have supposed to connect 3 fins as is shown in Figure 3.62. Figure 3.62 illustrates transfer characteristics dependence on the number of fins. In the case of I-V output characteristics, drain current increases with the increase of the number of fins as shown in the Figure 3.63. From Figures 3.63 and 3.64, it can be observed that 3 times of the drain current–and transconductance are approximately obtained in the three-fin device compared with that of in

the single-fin device at a fixed gate voltage and drain voltage, respectively. It should be noticed that the transconductance decreases rapidly with increasing positive V_{gs} for 3C-SiC channel materials. The maximum transconductance values increase with the number of Fins and decrease for increasing lengths [16].

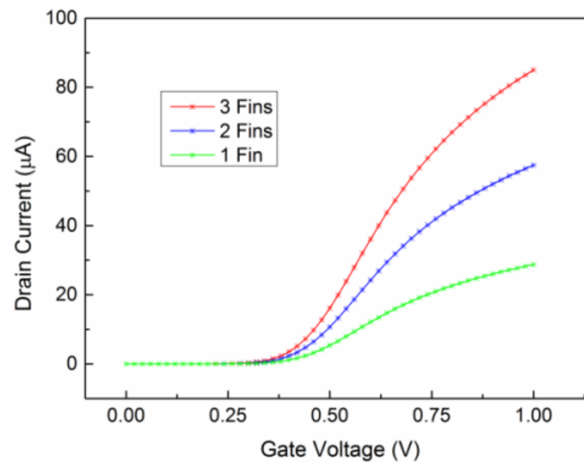

Figure 3.62 I_{ds}-V_{gs} characteristics on a linear scale for three n-transistors with different numbers of fins at V_{ds} = 0.2 V.

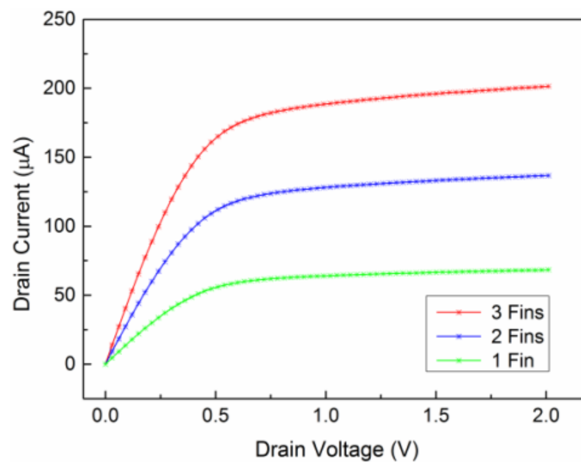

Figure 3.63 I_{ds}-V_{ds} characteristics for three n-transistors with different numbers of fins at V_{gs} = 1 V.

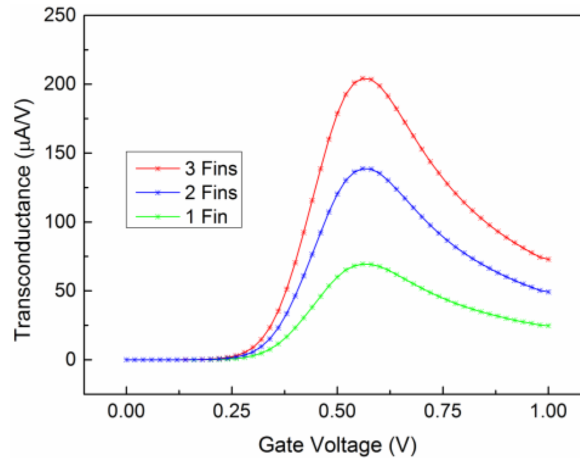

Figure 3.64 Transconductance versus V_{gs} for three n-transistors with different numbers of fins at V_{ds} = 0.2 V.

In this chapter, n-FinFET structure analysis and comparison to some manipulation parameter such variation of gate length, fin-thickness, gate dielectric materials, gate work function, and temperature were presented by numerical simulation. Furthermore, we have analysed the influence of quantum effect on the performance of n-FinFET for different gate lengths. The threshold voltage, subthreshold slope, transconductance, drain induced barrier lowering, leakage current, on-current, and On/Off current ratio have been analysed. A proper trading of fin width and gate work function improves short channel effects. The newly proposed transistor structure is compatible with current manufacturing process, which exhibited good performance characteristics down to 8 nm. The n-FinFET device with 8 nm gate length shows an improved drain current and an increase in transconductance. As a result, n-FinFET with ZrO_2 as gate dielectric material can be considered as a promising device for future semiconductor industry. With the CMOS processing technology already reached less than 22 nm regime, manufacturing n-FinFET devices should not be too complicated in future. Thus, for thin-film silicon on insulator or FinFET devices, the gate work function such as the FinFET technology is the most favorable technique for low-power subthreshold analog applications. We conclude that this study by looking the recent works produce different results which may be useful to the further manufacturing process.

Conclusion

The main goal of this thesis was to deal with using Virtual Wafer Fab software package accurately simulates semiconductor devices and their operation and make a comparative study between the results. The simulation process was performed in two different devices, a double-gate FinFET and a tri-gate FinFET one. Three dimensional numerical simulations using Silvaco^{TM} was performed to analyse the effect of various device parameters. Each time parameters of the device were altered, the simulated performance each device responded according to the equations and characteristics that would be expected from an actual, physical device. This accurate performance on parameters that can be calculated is helpful assuring the reliability of the program's simulations.

The overall goal of this research work was the optimization of semiconductor devices, and this objective was achieved. The performance of each of two devices was improved based on a low power, high-speed application. The threshold voltage of each device was lowered, and the transconductance was increased for each application, allowing for lowered operating voltages and increased switching speed. Through the course of this work, it has been shown that device performance can be controlled through the careful variation of device parameters and fabrication methods.

Generally, Silicon is a well-known material (in Simulators) with anticipated behaviour and there are not many things that can change that. Especially, as far as meshing is concerned, it is not necessary to have a fine mesh to perform the calculations, only a regular one, which can save a lot of computational effort and computer run-time.

However, this research work does not take into account fabrication costs and the feasibility of the fabrication of some of these devices. This project shows the incredible performance potential for each of these devices. While the performance of each device was enhanced, no study was done on the feasibility of creating these devices in a real world fabrication environment. Some methods of fabrication may be too costly, or may involve the creation of device areas whose scale is far too small for current technology.

There are limitless amounts of further research that can be done using these software tools. One recommendation would be for fabrication companies to use this software to determine the performance increases that would come from making certain fabrication methods more cost effective. This software package could be invaluable to a company desiring to improve current semiconductor technology. It would allow them to determine the most performance beneficial improvements that can be made to these devices before actual fabrication methods are devised, allowing for a cost vs. benefits projection for research and development.

However there are limits to what the simulation software can do. Since these programs are computer simulations, and not physical devices, some device variation due to fabrication methods and certain unexpected physical interactions on these devices have the possibility of not being properly simulated in new technology. These programs do simulate responses based on the physics of different elements present in the created devices, but they

are limited to the programed responses and interactions. For this reason, these simulations should be used as a guideline when researching new technology, not as a complete replacement for the fabrication of physical prototype devices. This simulation software has great potential to improve research, fabrication methods, and design goals for new semiconductor devices, but it needs to be used wisely with the advantages and limitations of the software in mind.

Finally, a great asset of Silvaco is a parametric design wizard which makes the whole procedure user-friendlier, since it is in the user's discretion to declare the value of each parameter according to the project's needs and finally, it has a better description of the physical models.

Future work

This thesis has provided greater understanding of the nanoscale n-FinFETs device and their parameters, there is still considerably more to learn. In addition, low frequency (1/f) noise measurements and their modelling on the FinFETs may provide further insight into the role of oxide charge trapping for corroboration with the mobility data. Little has been published in these areas.

The impact of the high-κ/metal gate is still a hot topic amongst researchers, and there would be scope to further improve the model for remote charge scattering proposed here, especially with regard to analysing "higher-κ" dielectrics and metal gate combinations.

It is recommended for further research to study different materials (other than Silicon) like Silicon Carbide, tests on variability and noise and user-defined physical models or new structures. There is also considerable scope for further research on strained SiGe or pure Ge based FinFETs. Such devices could have significantly higher mobility and be of relevance for future technology nodes.

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